

# LCFC Confidential

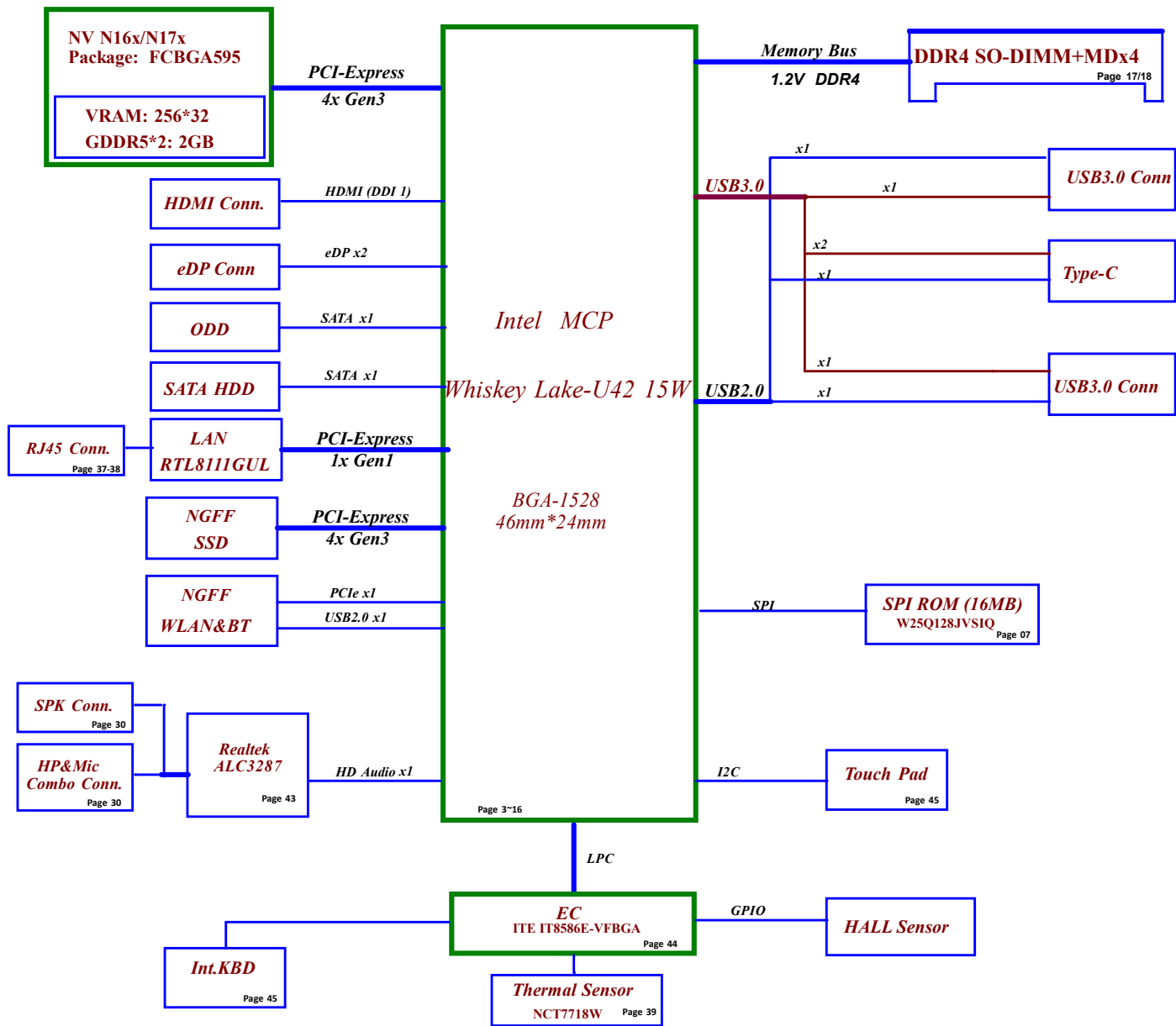
## FG540 MB Schematics Document

WHL U42 with DDR4 + Nvidia N16V-GM/N17S-G0

2018-07

REV: 0.1

Security Classification		LC Future Center Secret Data		Title			
Issued Date		2015/08/20	Deciphered Date	2016/08/20	Cover Page		
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Voltage Rails ( O --> Means ON , X --> Means OFF )

Power Plane				
State	V20B+	+3VALW +5VALW +3VALW_PCH +1.8VALW +1.05VALW	+1.2V +2.5V_DDR +VCCST	+5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS
S0	O	O	O	O
S3	O	O	O	X
S3 Battery only	O	O	O	X
S5 S4 AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE	SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

HSIO PORT	Function
USB3.0	1 USB3.0 Conn Right
	2 USB3.0 Conn Left
	3 NC
	4 NC
	5 NC
	6 NC
USB2.0	1 USB3.0 Conn Left
	2 NC
	3 USB3.0 Conn Right
	4 Finger Print
	5 Card reader
	6 NC
PCIE	7 Camera
	8 NC
	9 NC
	10 Bluetooth
	5~8 X4 DGPU
	9 Giga LAN
	10 NC
	11 SATA HDD
	12 WLAN
	13~16 X4 PCIE/SATA SSD

BOM Structure	BTO Item
@	Un-stuff
14@	For 14" part
15@	For 15" part
YOGA@	For YOGA530 part
530@	For 530S part
CD@	For C cost down
EMC@	For EMC part
EMC_15@	For EMC 15" part
EMC_NS@	For EMC un-stuff part
EMC_PX@	For EMC PX part
EMC_PXNS@	For EMC PX nu-stuff part
ME@	For ME part
OPT@	For NV GPU part
OPTN16@	For NV N16S-GTR GPU part
OPTN17@	For NV N17S-G1 GPU part
TS@	For touch screen part
TP@	For Touch Pad Part
UMA@	For UMA part

SMBUS Control Table

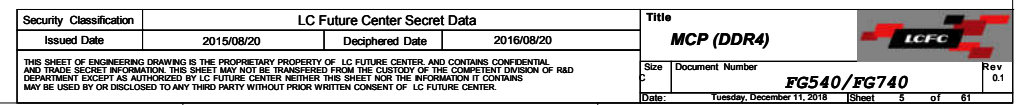
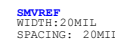
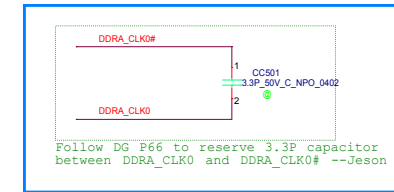
	SOURCE	BATT	Charger	DGPU	IT8586E	Memory Down	PCH	PMIC	SODIMM	Thermal Sensor	WLAN WiMAX
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL_EC	V	V	X	V +3VL_EC	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	X	X	V +3VG_AON	V +3VS	X	V +3VALW_PCH	X	X	V	X
EC_SMB_CK3 EC_SMB_DA3	IT8586E +3VL_EC	X	X	X	V +3VL_EC	X	X	V	X	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	X	X	V +3VALW_PCH	X	V +3VS	X	V +3VS

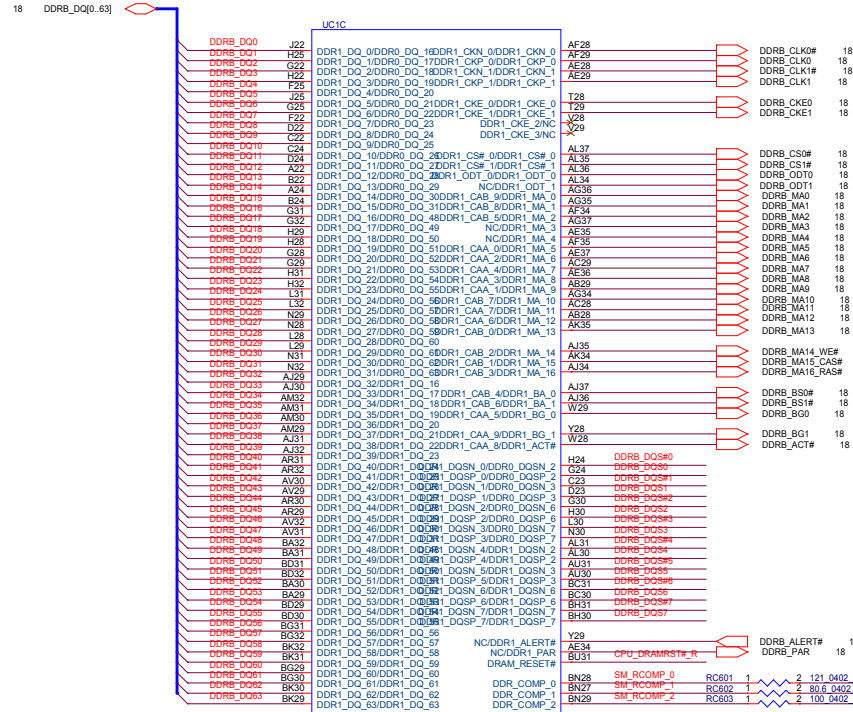
EC SMBus1 address      EC SMBus2 address      EC SMBus3 address      PCH SM Bus address

Device	Address	Device	Address	Device	Address	Device	Address
Smart Battery	need to update	Thermal Sensor(NCT7718W)	1001_100xb	PMIC	need to update	DDR4 SODIMM	need to update
Charger	0001 0010 b	PCH	need to update			Wlan	Reserved
		DGPU	need to update				

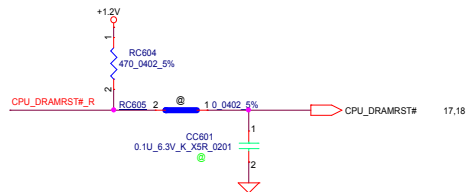


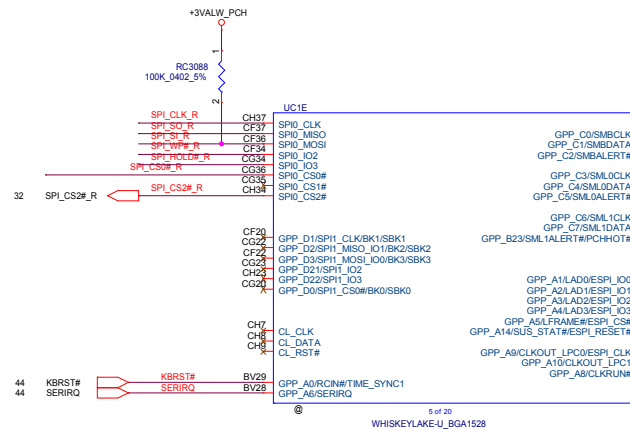




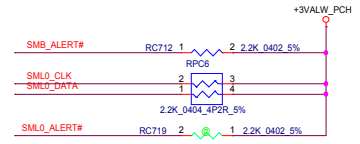


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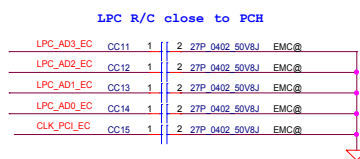
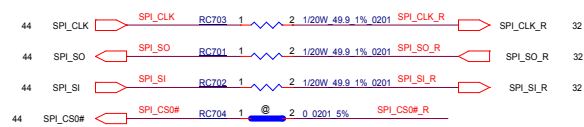




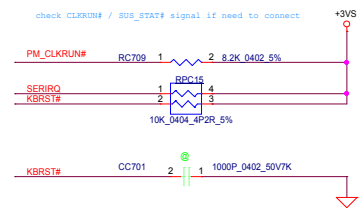
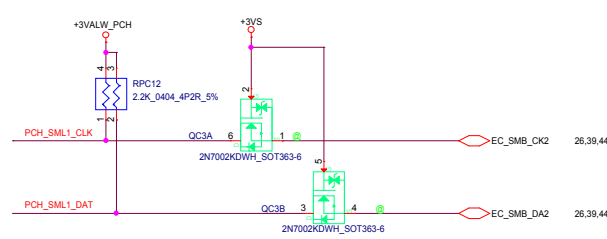
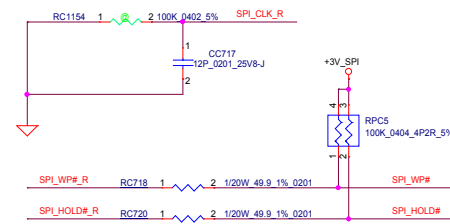
TLS Confidentiality (Rising edge of RSMRST#)  
This signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security(TLS) cipher suite (no confidentiality). (Default)  
1 = Enable Intel ME Crypto Transport Layer Security(TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS.  
Notes:  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.



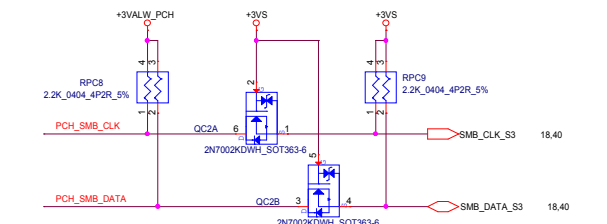
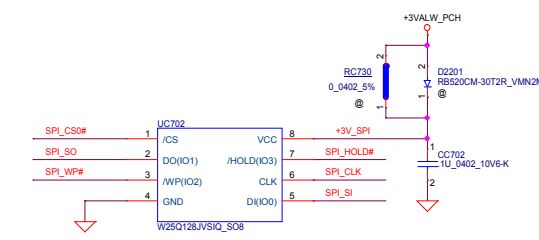
eSPI or LPC (Rising edge of RSMRST#)  
This signal has a weak internal pull-down.  
0 = LPC is selected for EC. (Default)  
1 = eSPI is selected for EC.  
Notes:  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. This signal is in the primary well.



Intel DCI-OOB (Rising edge of RSMRST#)  
This signal has an internal pull-down.  
0 = Disable Intel DCI-OOB (Default)  
1 = Enable Intel DCI-OOB  
Notes:  
1. The internal pull-down is disabled after RSMRST# de-asserts.  
2. When used as PCHHOT# and strap low, a 150K pull-up is needed to ensure it does not override the internal pull-down strap sampling.  
This signal is in the primary well.



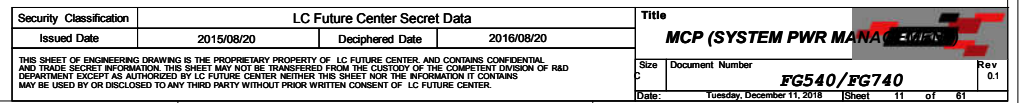
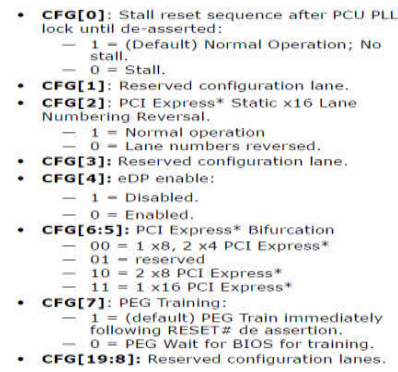
SPI0\_MOSI: Reserved (Rising edge of RSMRST#)  
SPI0\_IO2: Reserved (Rising edge of RSMRST#)  
SPI0\_IO3: Reserved (Rising edge of RSMRST#)  
External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.



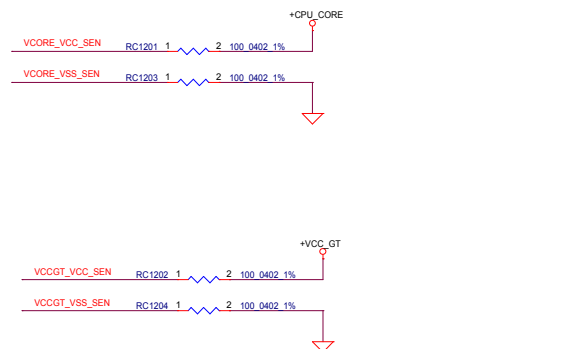
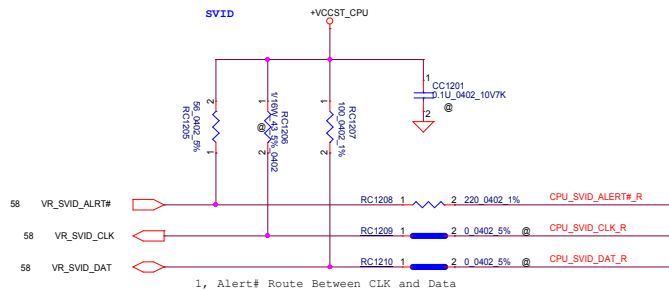




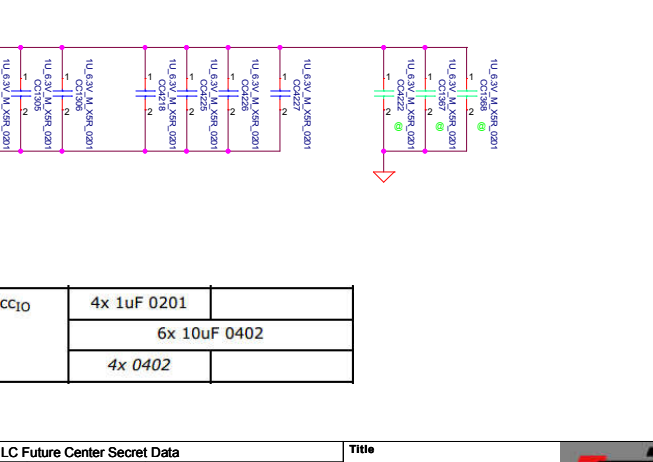
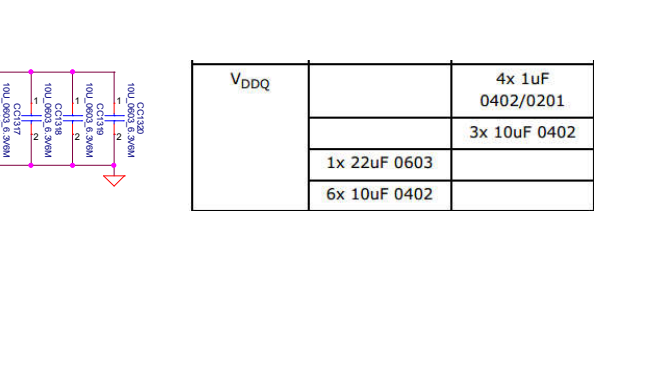
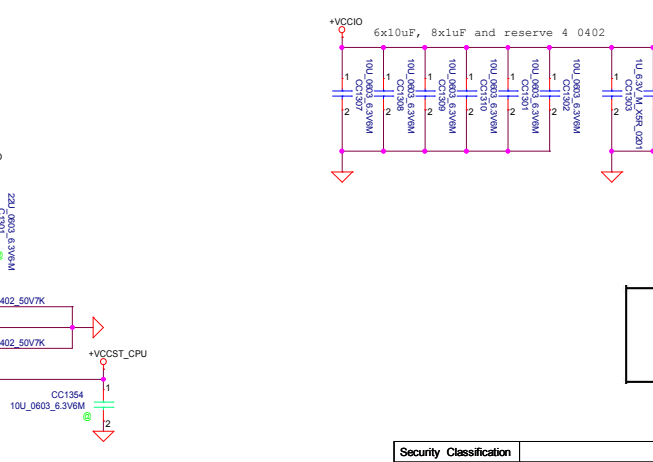
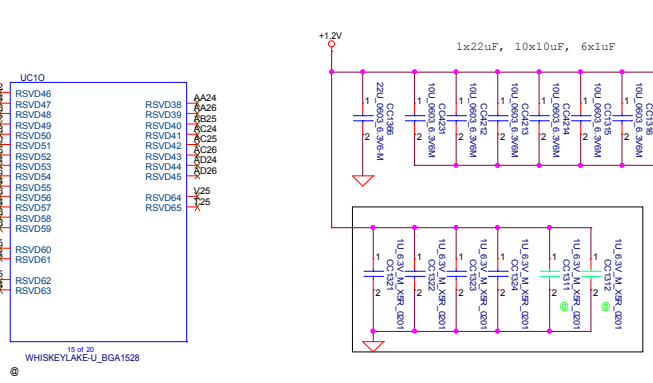
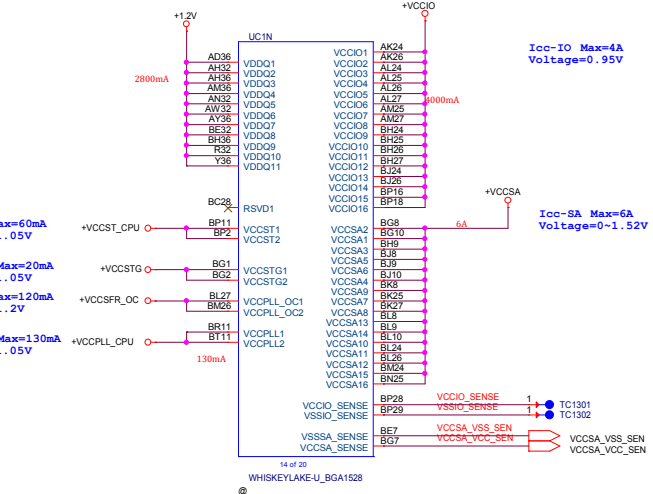
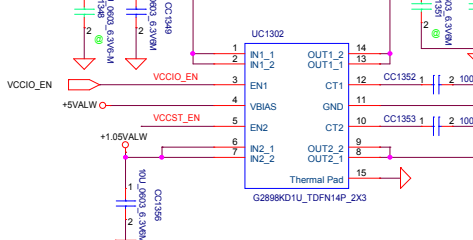
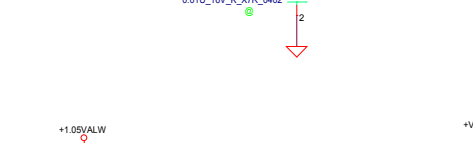
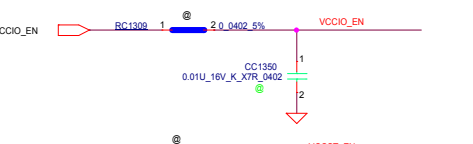
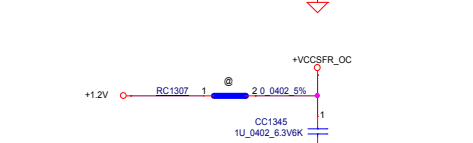
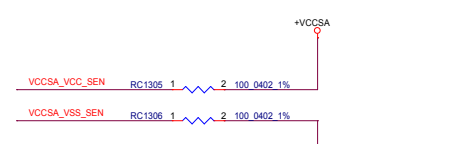
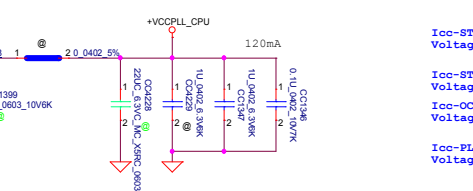
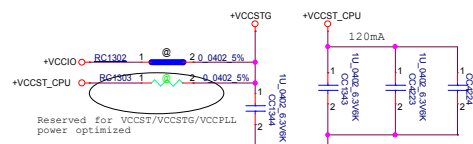








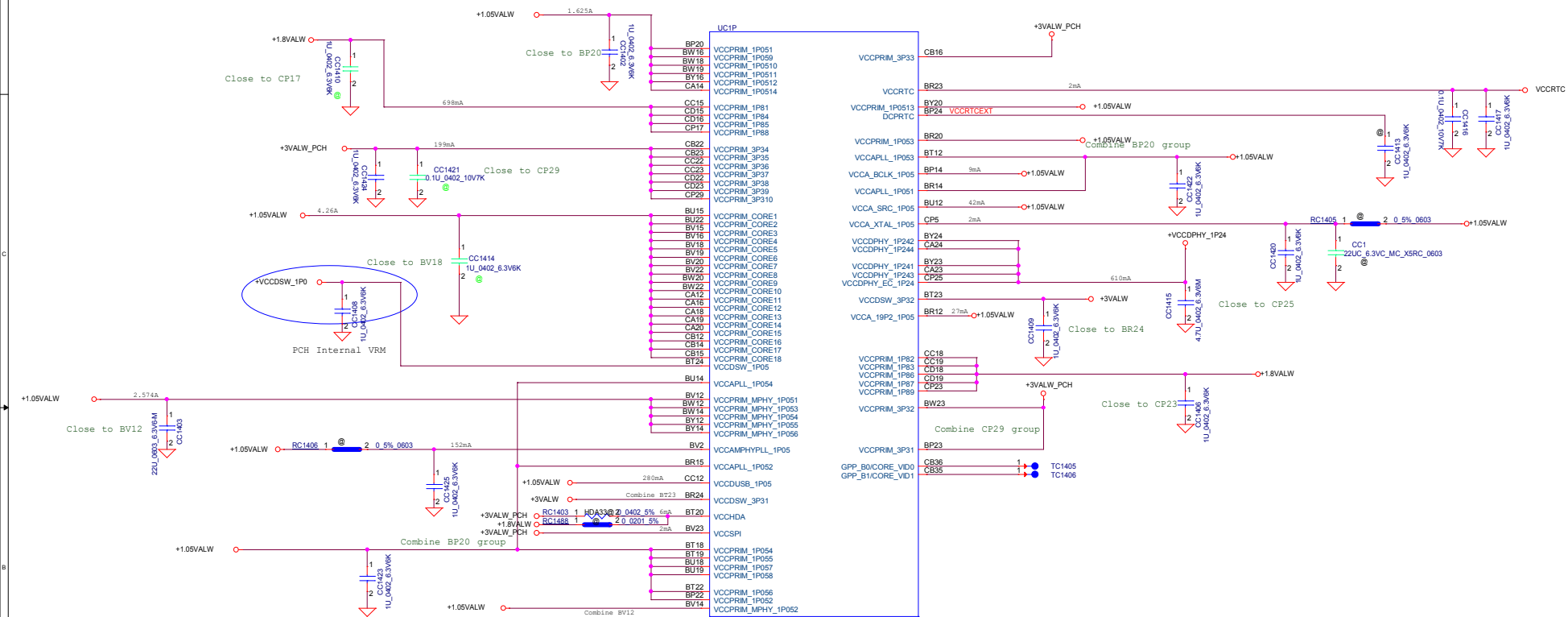





V <sub>DDQ</sub>		4x 1uF 0402/0201
		3x 10uF 0402
	1x 22uF 0603	
	6x 10uF 0402	

V <sub>CCIO</sub>	4x 1uF 0201
	6x 10uF 0402
	4x 0402

Refer to DOC# 566439-P58



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Issued Date		2015/08/20		Deciphered Date			2016/08/20		MCP (PCH PWR)			
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UC1S		
BT35	VSS_145	VSS_217
D6	VSS_146	VSS_218
AL32	VSS_147	VSS_219
BT36	VSS_148	VSS_220
D8	VSS_149	VSS_221
AL7	VSS_150	VSS_222
D9	VSS_151	VSS_223
AM10	VSS_152	VSS_224
BU11	VSS_153	VSS_225
E23	VSS_154	VSS_226
AM28	VSS_155	VSS_227
E27	VSS_156	VSS_228
AM33	VSS_157	VSS_229
BU23	VSS_158	VSS_230
E29	VSS_159	VSS_231
AM35	VSS_160	VSS_232
BU24	VSS_161	VSS_233
E31	VSS_162	VSS_234
BU25	VSS_163	VSS_235
E33	VSS_164	VSS_236
AN25	VSS_165	VSS_237
BU7	VSS_166	VSS_238
E9	VSS_167	VSS_239
AN28	VSS_168	VSS_240
BV11	VSS_169	VSS_241
F12	VSS_170	VSS_242
AN29	VSS_171	VSS_243
F15	VSS_172	VSS_244
AN30	VSS_173	VSS_245
F18	VSS_174	VSS_246
AN31	VSS_175	VSS_247
BV3	VSS_176	VSS_248
E2	VSS_177	VSS_249
AN7	VSS_178	VSS_250
BV11	VSS_179	VSS_251
F21	VSS_180	VSS_252
AN8	VSS_181	VSS_253
BV33	VSS_182	VSS_254
F24	VSS_183	VSS_255
BV4	VSS_184	VSS_256
F3	VSS_185	VSS_257
AP3	VSS_186	VSS_258
BW11	VSS_187	VSS_259
F4	VSS_188	VSS_260
AP33	VSS_189	VSS_261
BW15	VSS_190	VSS_262
C31	VSS_191	VSS_263
AP36	VSS_192	VSS_264
C27	VSS_193	VSS_265
AP4	VSS_194	VSS_266
G33	VSS_195	VSS_267
AR28	VSS_196	VSS_268
G36	VSS_197	VSS_269
AT33	VSS_198	VSS_270
BW24	VSS_199	VSS_271
G9	VSS_200	VSS_272
AT35	VSS_201	VSS_273
H21	VSS_202	VSS_274
AT36	VSS_203	VSS_275
BW7	VSS_204	VSS_276
H27	VSS_205	VSS_277
AT4	VSS_206	VSS_278
BY11	VSS_207	VSS_279
AU10	VSS_208	VSS_280
BY15	VSS_209	VSS_281
H9	VSS_210	VSS_282
AU28	VSS_211	VSS_283
BY22	VSS_212	VSS_284
J12	VSS_213	VSS_285
AU29	VSS_214	VSS_286
J15	VSS_215	VSS_287
	VSS_216	VSS_288
	VSS_217	VSS_289

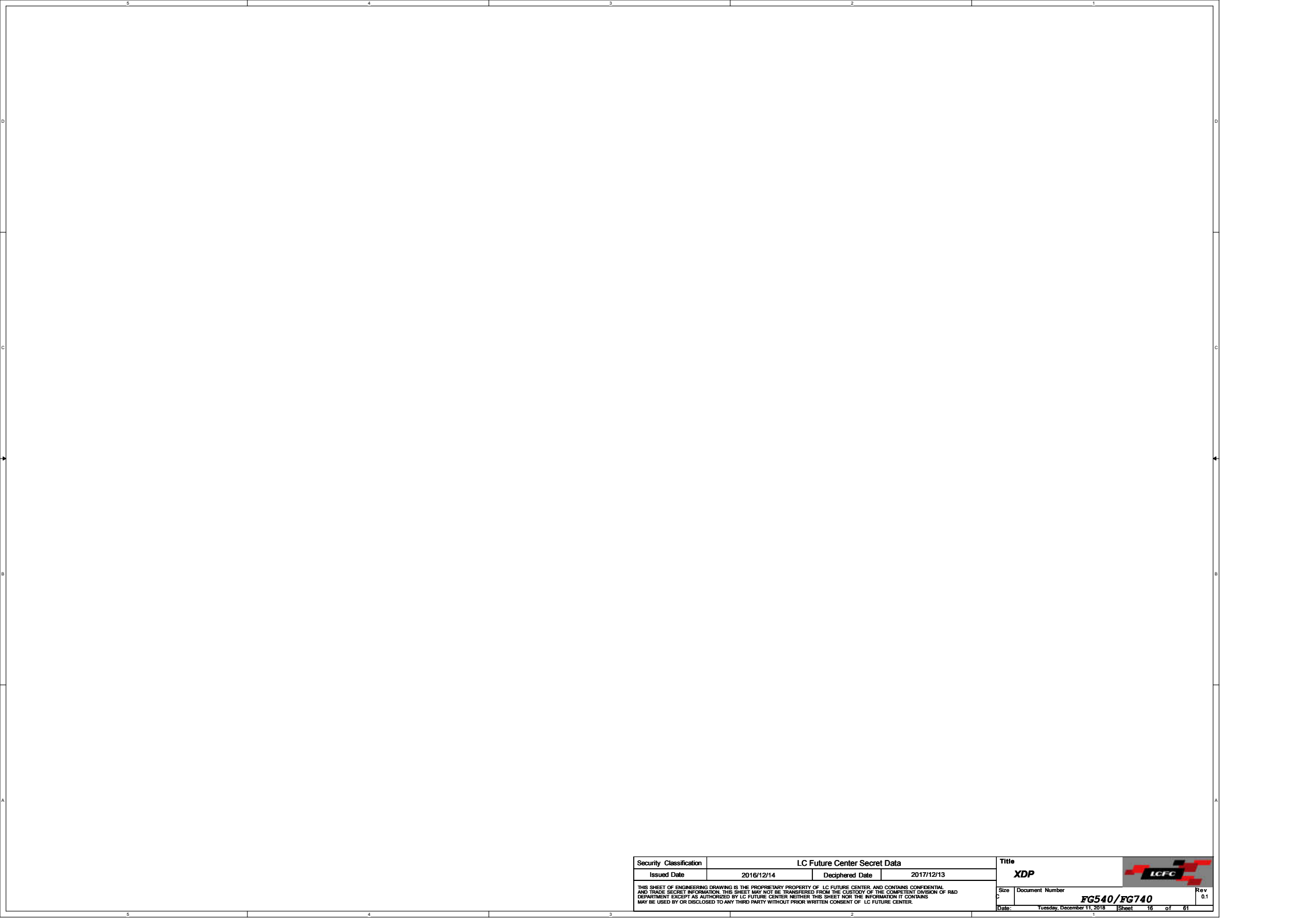
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UC1T		
N6	VSS_290	VSS_362
B37	VSS_291	VSS_363
B10	VSS_292	VSS_364
B5	VSS_293	VSS_365
CB31	VSS_294	VSS_366
P33	VSS_295	VSS_367
Q34	VSS_296	VSS_368
B7	VSS_297	VSS_369
P33	VSS_298	VSS_370
Q34	VSS_299	VSS_371
B9	VSS_300	VSS_372
P36	VSS_301	VSS_373
Q34	VSS_302	VSS_374
BA10	VSS_303	VSS_375
BA28	VSS_304	VSS_376
P7	VSS_305	VSS_377
BA3	VSS_306	VSS_378
CC20	VSS_307	VSS_379
B27	VSS_308	VSS_380
BB3	VSS_309	VSS_381
CC25	VSS_310	VSS_382
R28	VSS_311	VSS_383
BB33	VSS_312	VSS_384
CC28	VSS_313	VSS_385
R28	VSS_314	VSS_386
BB36	VSS_315	VSS_387
CC31	VSS_316	VSS_388
R30	VSS_317	VSS_389
BB4	VSS_318	VSS_390
CC34	VSS_319	VSS_391
R31	VSS_320	VSS_392
BB5	VSS_321	VSS_393
CC37	VSS_322	VSS_394
R32	VSS_323	VSS_395
BB6	VSS_324	VSS_396
CC40	VSS_325	VSS_397
R33	VSS_326	VSS_398
BB7	VSS_327	VSS_399
CC43	VSS_328	VSS_400
R34	VSS_329	VSS_401
BB8	VSS_330	VSS_402
CC46	VSS_331	VSS_403
R35	VSS_332	VSS_404
BB9	VSS_333	VSS_405
CC49	VSS_334	VSS_406
R36	VSS_335	VSS_407
BB10	VSS_336	VSS_408
CC52	VSS_337	VSS_409
R37	VSS_338	VSS_410
BB11	VSS_339	VSS_411
CC55	VSS_340	VSS_412
R38	VSS_341	VSS_413
BB12	VSS_342	VSS_414
CC58	VSS_343	VSS_415
R39	VSS_344	VSS_416
BB13	VSS_345	VSS_417
CC61	VSS_346	VSS_418
R40	VSS_347	VSS_419
BB14	VSS_348	VSS_420
CC64	VSS_349	VSS_421
R41	VSS_350	VSS_422
BB15	VSS_351	VSS_423
CC67	VSS_352	VSS_424
R42	VSS_353	VSS_425
BB16	VSS_354	VSS_426
CC70	VSS_355	VSS_427
R43	VSS_356	VSS_428
BB17	VSS_357	VSS_429
CC73	VSS_358	VSS_430
R44	VSS_359	VSS_431
BB18	VSS_360	VSS_432
CC76	VSS_361	VSS_433

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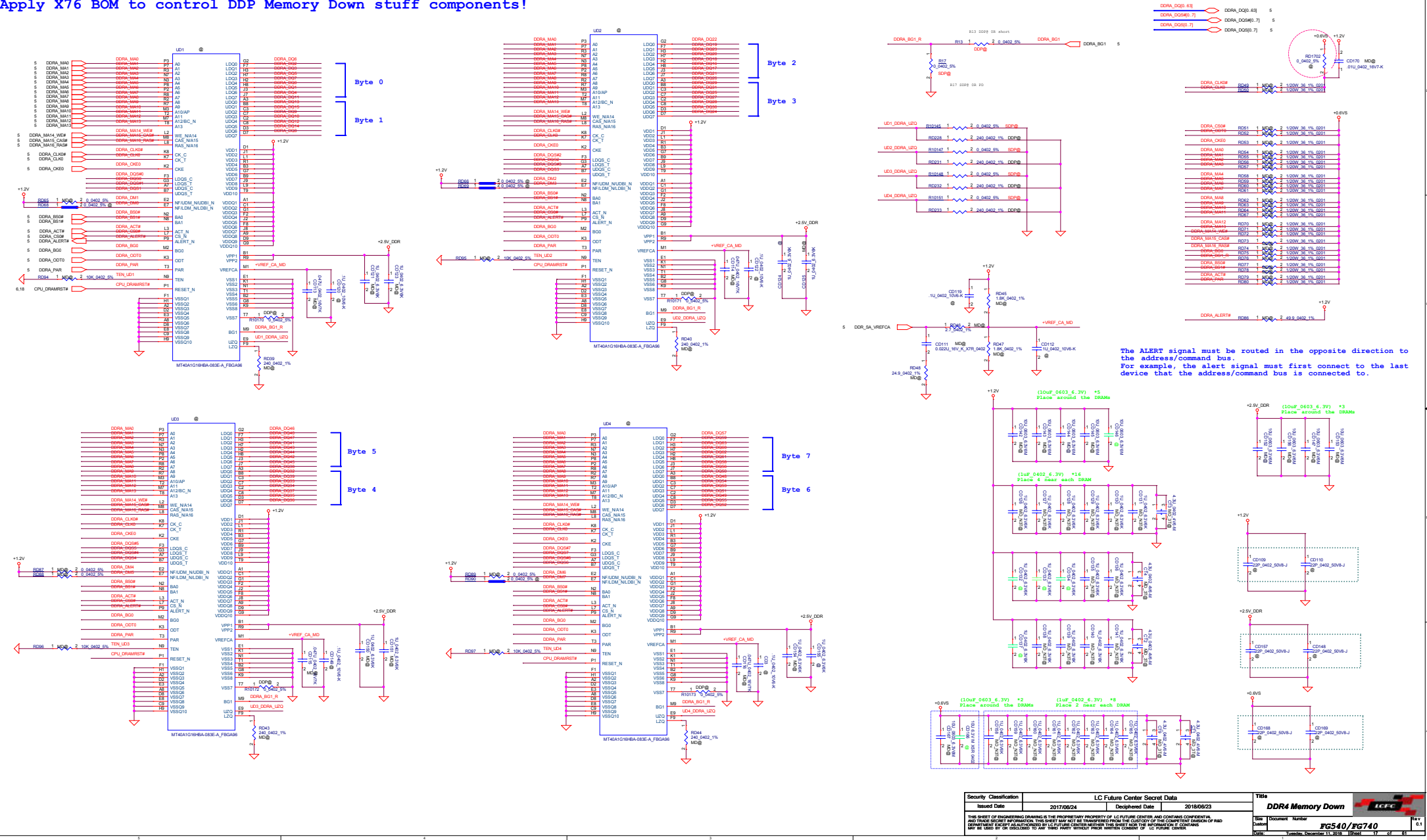
UC1R		
CR34	VSS_1	VSS_73
BL7	VSS_2	VSS_74
AE25	VSS_3	VSS_75
CM6	VSS_4	VSS_76
AE27	VSS_5	VSS_77
CM9	VSS_6	VSS_78
AE30	VSS_7	VSS_79
CM10	VSS_8	VSS_80
AE32	VSS_9	VSS_81
CM11	VSS_10	VSS_82
AE34	VSS_11	VSS_83
CM12	VSS_12	VSS_84
AE36	VSS_13	VSS_85
CM13	VSS_14	VSS_86
AE38	VSS_15	VSS_87
CM14	VSS_16	VSS_88
AE40	VSS_17	VSS_89
CM15	VSS_18	VSS_90
AE42	VSS_19	VSS_91
CM16	VSS_20	VSS_92
AE44	VSS_21	VSS_93
CM17	VSS_22	VSS_94
AE46	VSS_23	VSS_95
CM18	VSS_24	VSS_96
AE48	VSS_25	VSS_97
CM19	VSS_26	VSS_98
AE50	VSS_27	VSS_99
CM20	VSS_28	VSS_100
AE52	VSS_29	VSS_101
CM21	VSS_30	VSS_102
AE54	VSS_31	VSS_103
CM22	VSS_32	VSS_104
AE56	VSS_33	VSS_105
CM23	VSS_34	VSS_106
AE58	VSS_35	VSS_107
CM24	VSS_36	VSS_108
AE60	VSS_37	VSS_109
CM25	VSS_38	VSS_110
AE62	VSS_39	VSS_111
CM26	VSS_40	VSS_112
AE64	VSS_41	VSS_113
CM27	VSS_42	VSS_114
AE66	VSS_43	VSS_115
CM28	VSS_44	VSS_116
AE68	VSS_45	VSS_117
CM29	VSS_46	VSS_118
AE70	VSS_47	VSS_119
CM30	VSS_48	VSS_120
AE72	VSS_49	VSS_121
CM31	VSS_50	VSS_122
AE74	VSS_51	VSS_123
CM32	VSS_52	VSS_124
AE76	VSS_53	VSS_125
CM33	VSS_54	VSS_126
AE78	VSS_55	VSS_127
CM34	VSS_56	VSS_128
AE80	VSS_57	VSS_129
CM35	VSS_58	VSS_130
AE82	VSS_59	VSS_131
CM36	VSS_60	VSS_132
AE84	VSS_61	VSS_133
CM37	VSS_62	VSS_134
AE86	VSS_63	VSS_135
CM38	VSS_64	VSS_136
AE88	VSS_65	VSS_137
CM39	VSS_66	VSS_138
AE90	VSS_67	VSS_139
CM40	VSS_68	VSS_140
AE92	VSS_69	VSS_141
CM41	VSS_70	VSS_142
AE94	VSS_71	VSS_143
CM42	VSS_72	VSS_144

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WHISKEYLAKE-U\_BGA1528

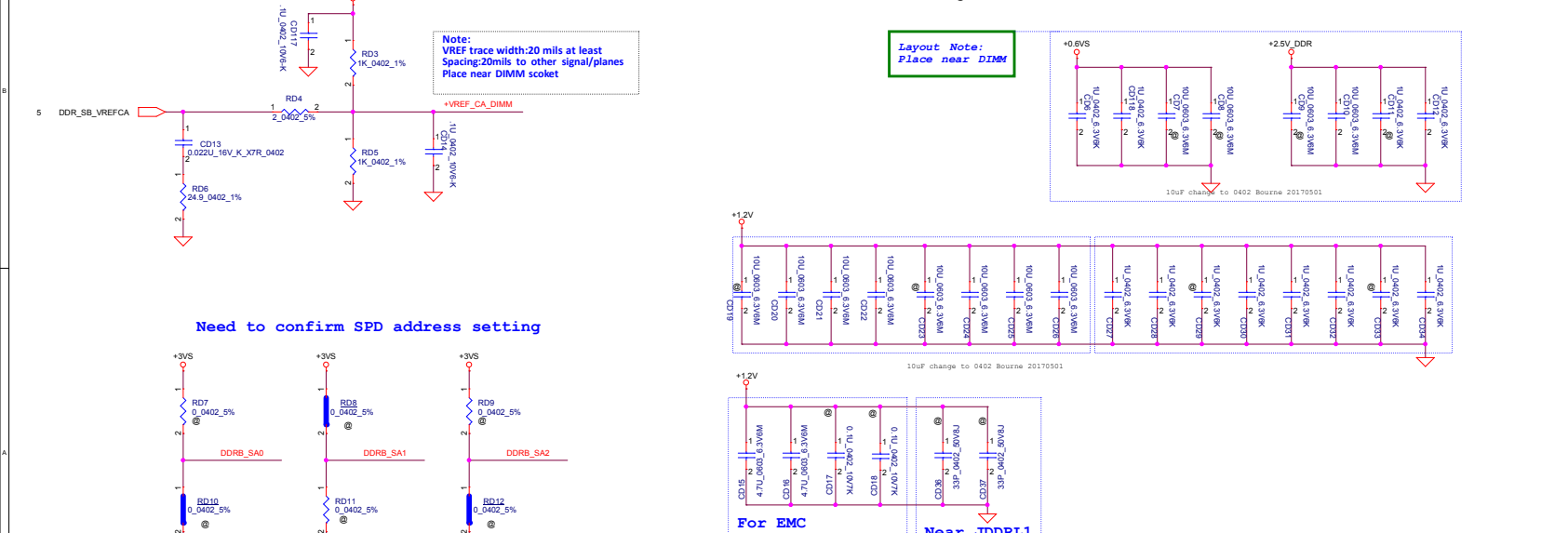
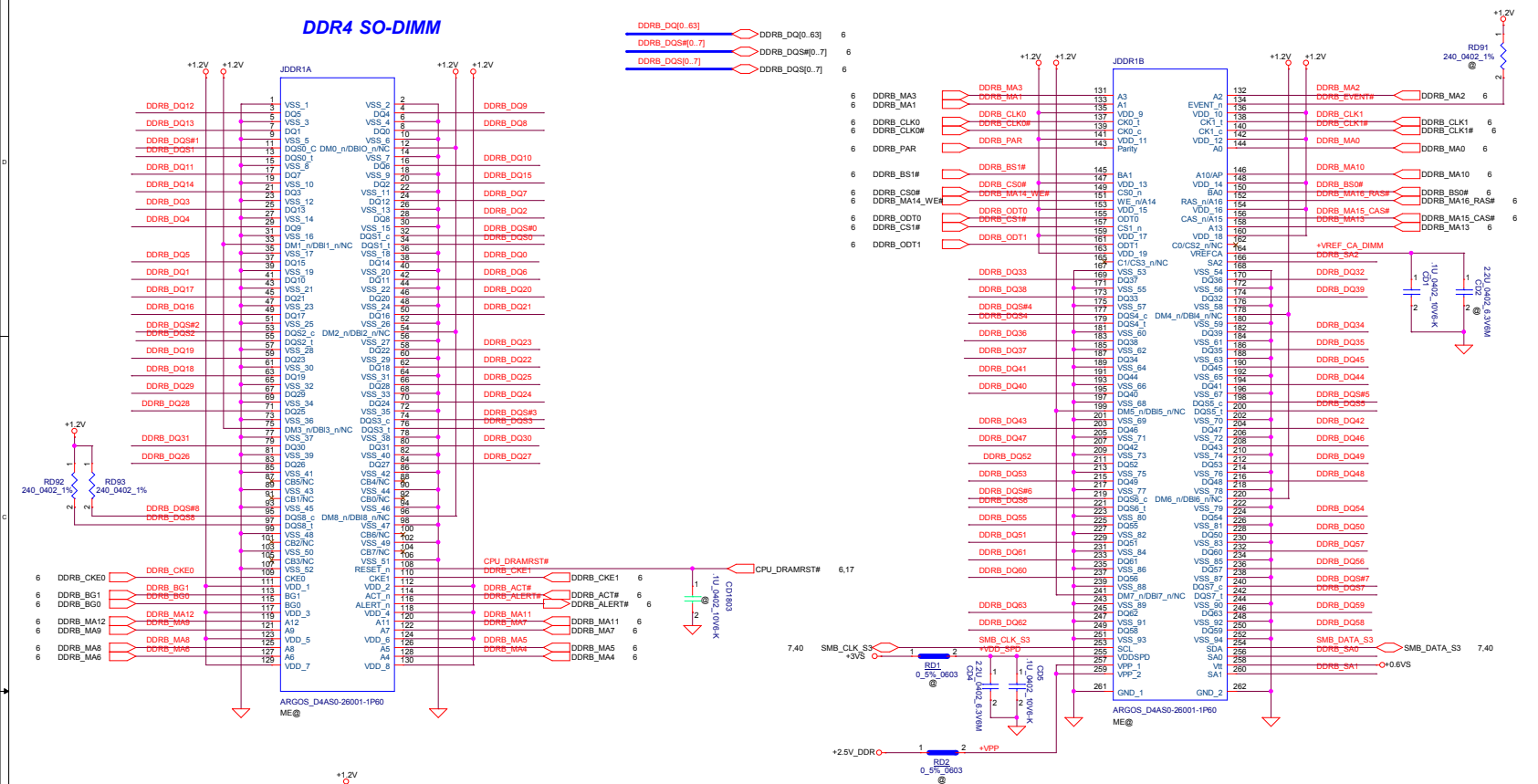


Security Classification		LC Future Center Secret Data		Title		
Issued Date		2016/12/14	Deciphered Date	2017/12/13	XDP	
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Size	Document Number				Rev	
C	FG540/FG740				0.1	
Date: Tuesday, December 11, 2018					Sheet 16 of 61	

Apply X76 BOM to control DDP Memory Down stuff components!



# DDR4 SO-DIMM



SPD Address = 0XA4(follow CRB)

Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/08/20	Deciphered Date	2016/08/20	DDR4 SO-DIMM	
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Size	Document Number	Rev			
	FC540/FC740	6.1			
Date	Tuesday, December 11, 2016	Sheet	18	of 61	

N16x GPIO

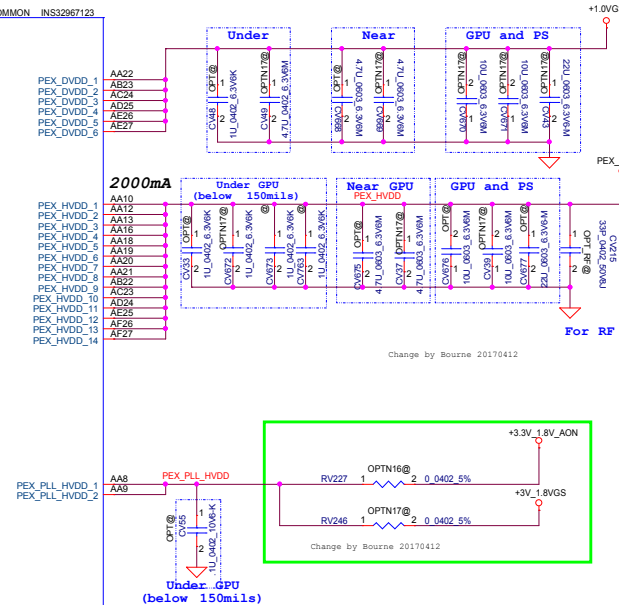
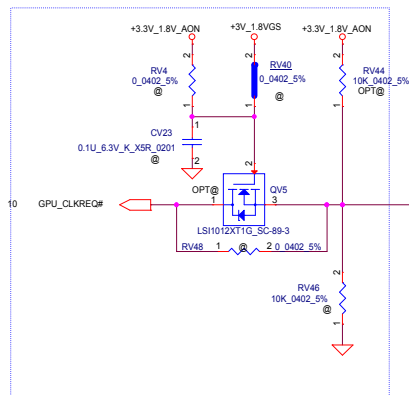
GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU Core VDD PWM control signal
GPIO1	OUT	N/A	FB Enable for GC6 2.0
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing--3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT		FBVREF_ALTV for GDDR5
GPIO11	OUT	-	
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

Products	GPU	Mem	Min Core Clk	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		(1.05V) (6)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)
N16S-GMR	16	1.6	849	TBD	19	TBD	2	TBD	4.2	TBD	800	TBD	60	TBD
N16S-GTR	18	1.7	967		26.5		2		4.2		800		60	

N16x Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS				
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			



PEX\_DVDD  
N16:+1.05VGS (recommend)  
+1.0VGS (Used)  
N17:+1.0VGS

PEX\_HVDD  
N16:+1.05VGS (recommend)  
+1.0VGS (Used)  
N17:+1.8VGS

PEX\_PLL HVDD  
N16:+3.3V AON  
N17:+1.8VGS

#### PEX\_DVDD/Q Decoupling

MLCC	N16	N17	location
1.0uF	1	1	Under
4.7uF	0	1	
4.7uF	1	2	
10uF	0	2	Midway
22uF	0	1	

#### PEX\_HVDD/Q Decoupling

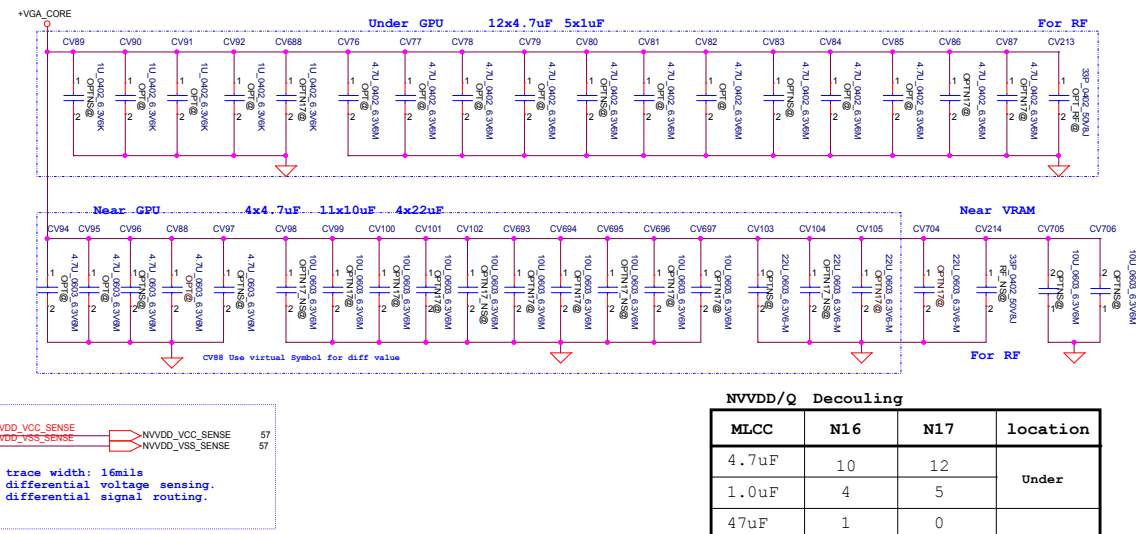
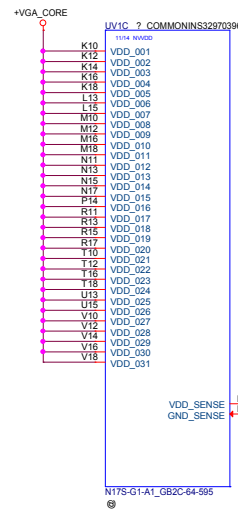
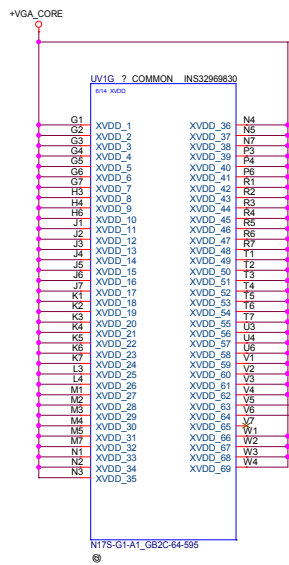
MLCC	N16	N17	location
1.0uF	1	4	Under
4.7uF	1	2	Near
10uF	1	2	Midway
22uF	1	1	

#### PEX\_PLL HVDD/Q Decoupling

MLCC	N16	N17	location
0.1uF	1	1	Near

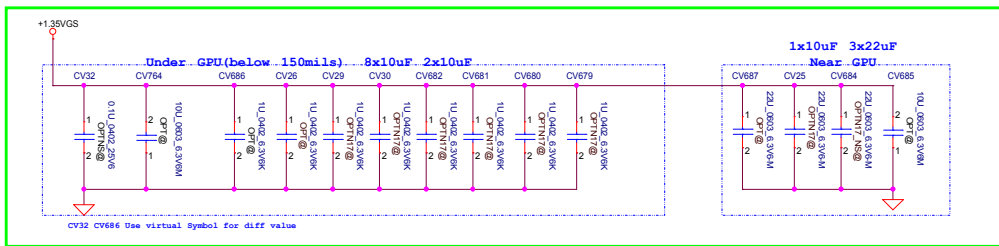
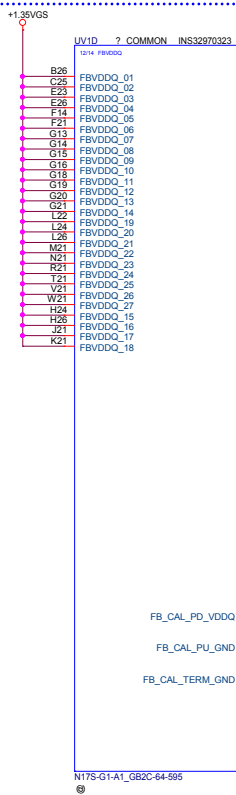






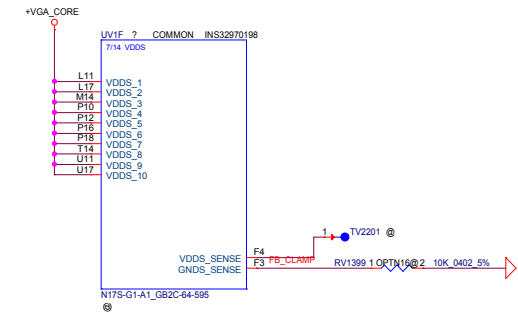
**NVVDV/Q Decoupling**

MLCC	N16	N17	location
4.7uF	10	12	Under
1.0uF	4	5	
47uF	1	0	Near
10uF	0	11	
22uF	1	4	
4.7uF	5	4	
330uF	1	2	

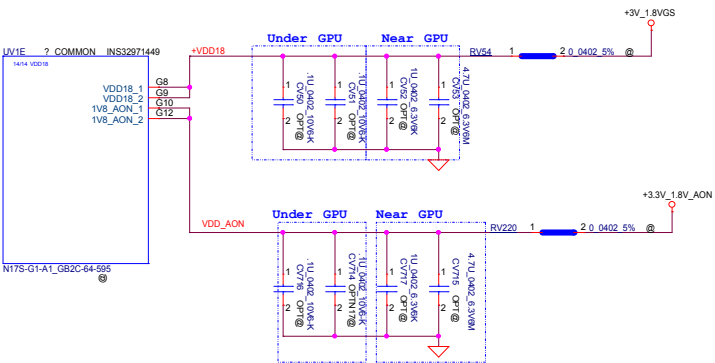


**FBVDD/Q Decoupling**

MLCC	N16	N17	location
0.1uF	2	0	Under
1.0uF	2	8	
4.7uF	2	0	Near
10uF	0	2	
10uF	1	1	
22uF	1	3	



CALIBRATION PIN	GDDR5
FB_CAL x_PD_VDDQ	40.2Ohm
FB_CAL x_PU_GND	40.2Ohm
FB_CAL xTERM_GND	60.4Ohm



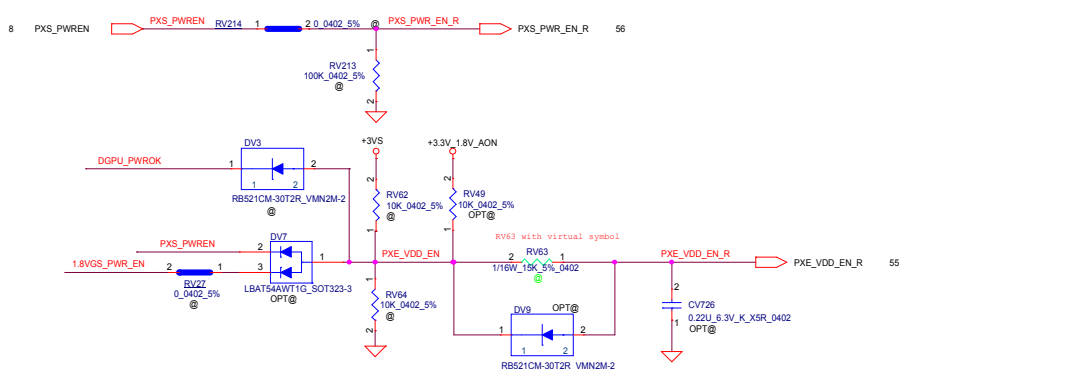
N16 3V3\_MAIN(N17 VDD\_18) Decoupling

MLCC	N16	N17	location
0.1uF	2	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

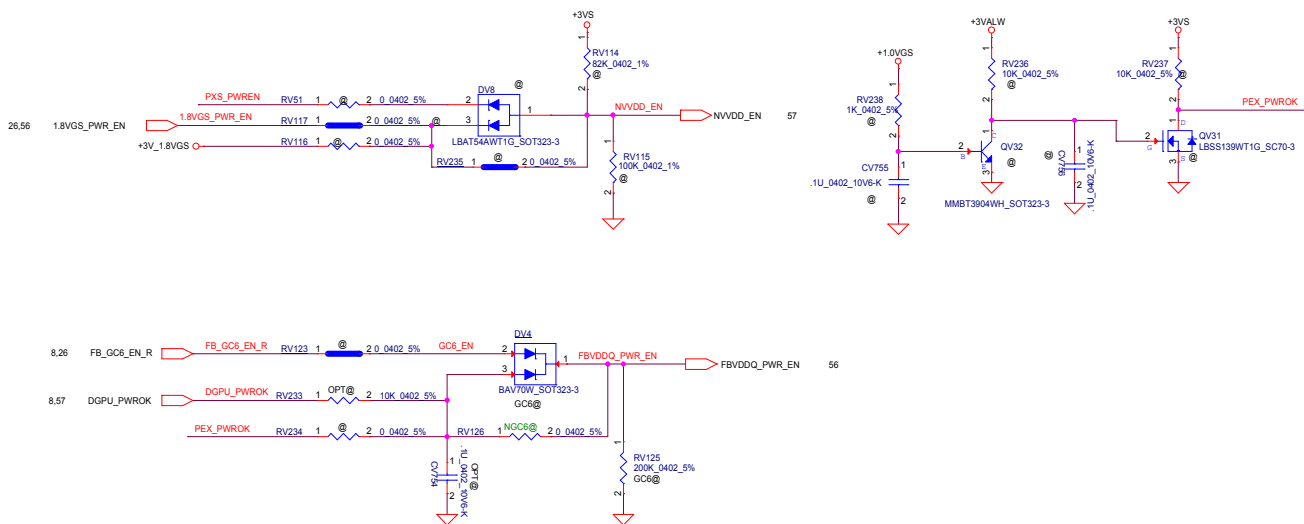
N16 3V3\_AON(N17 1V8\_AON) Decoupling

MLCC	N16	N17	location
0.1uF	1	2	Under
1.0uF	1	1	Near
4.7uF	1	1	

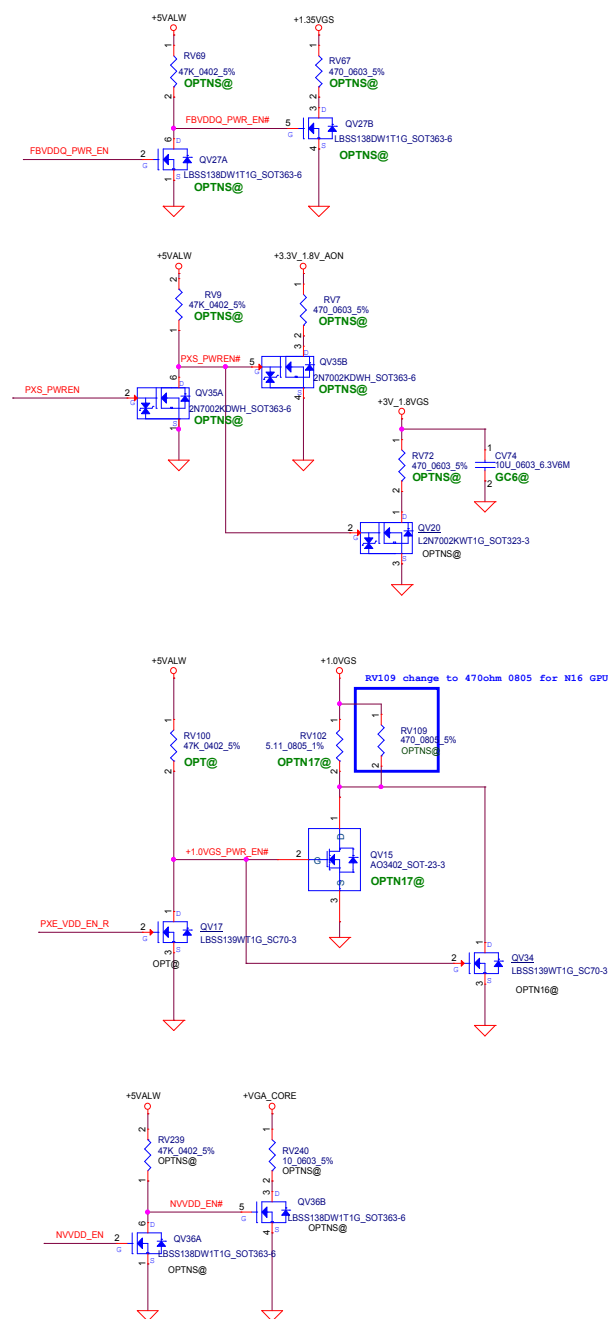
PXE\_VDD & 1V8\_AON

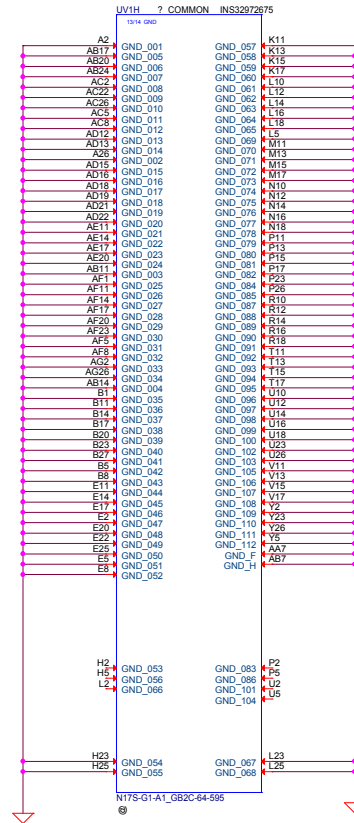


+1.8VG\_AON TO +1.8VGS

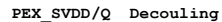


Discharge

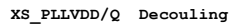




MLCC	N16	N17	location
1.0uF	1	NA	Under
1uF	1	NA	Near
4.7uF	1	NA	



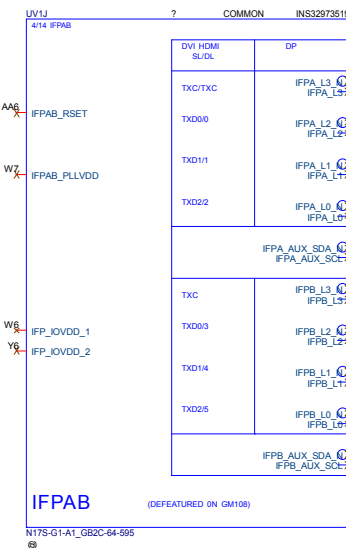
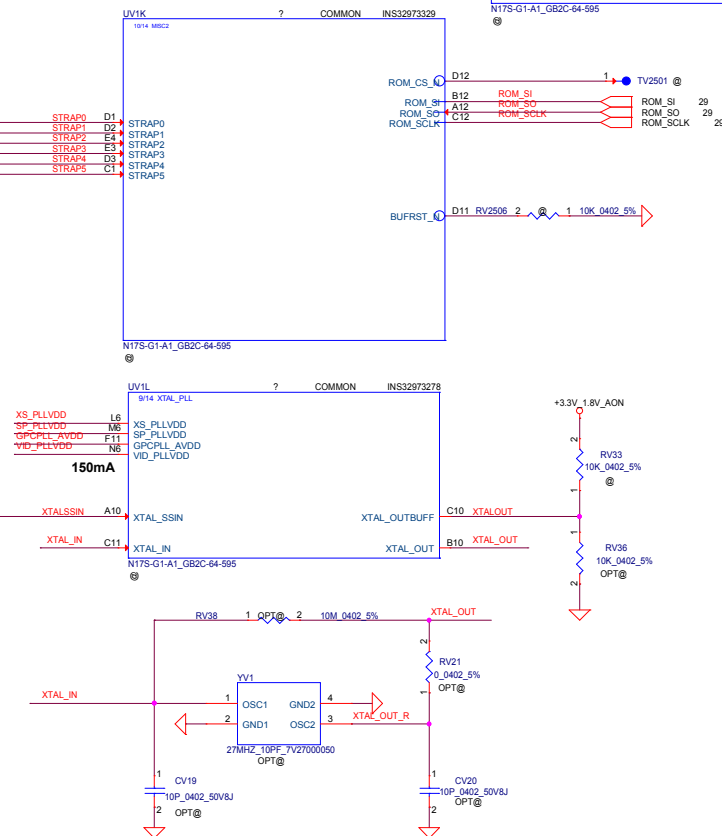
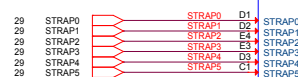
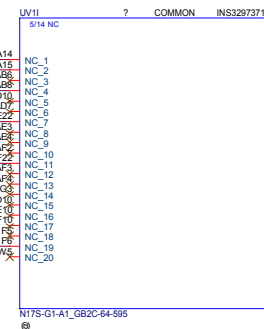
MLCC	N16	N17	location
4.7uF	2	NA	Near

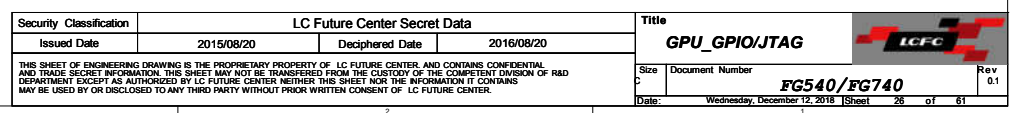
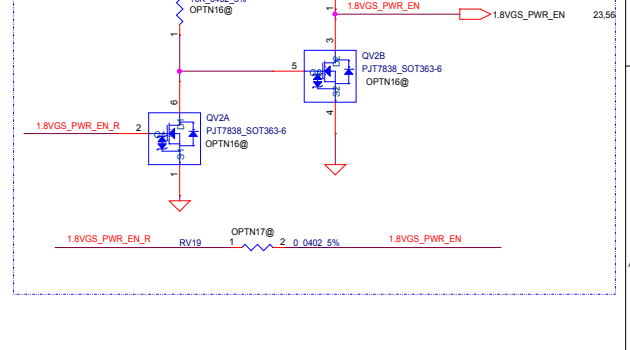


MLCC	N16	N17	location
0.1uF	1	1	Under
22uF	1	0	Near

MLCC	N16	N17	location
0.1uF	2	2	Under
10uF	1	0	Near
47uF	1	0	

MLCC	N16	N17	location
0.1uF	NA	1	Under
4.7uF	NA	1	Near
22uF	NA	1	



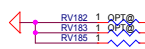
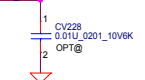


# Lower 32 bits

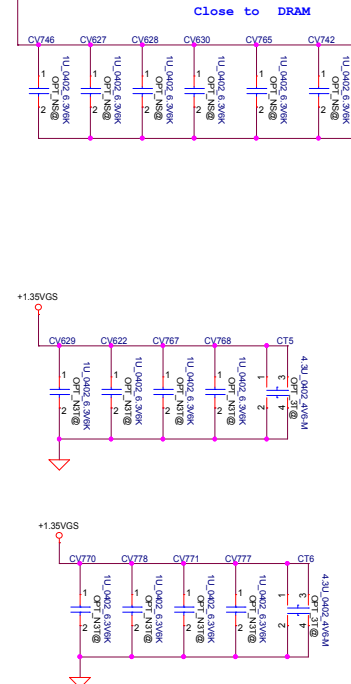
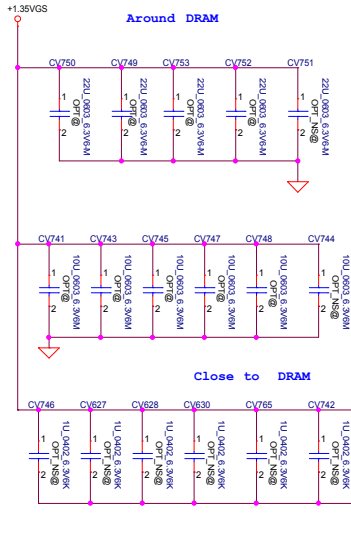
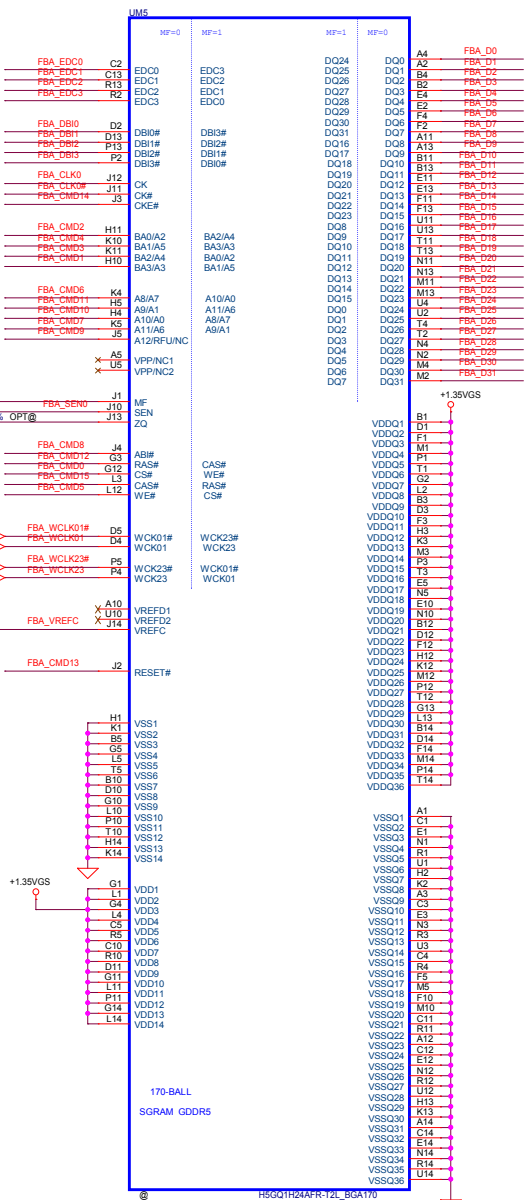
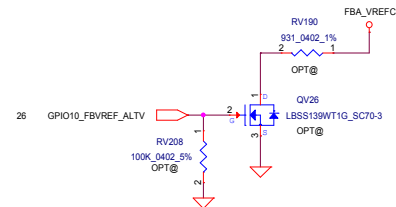
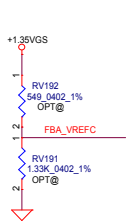
## MF=0 No Mirror

21.28 FBA\_D[0..63]  
21.28 FBA\_CMD[31..0]  
21.28 FBA\_EDC[7..0]  
21.28 FBA\_DB[7..0]

21 FBA\_CLK0  
21 FBA\_CLK0#

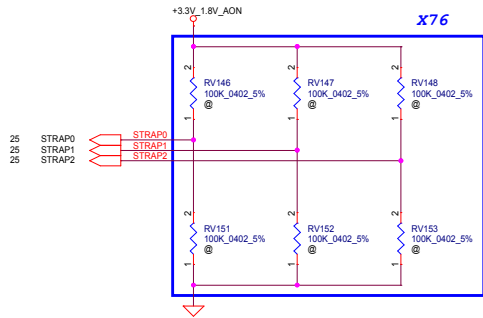


21 FBA\_WCLK01#  
21 FBA\_WCLK01  
21 FBA\_WCLK23#  
21 FBA\_WCLK23

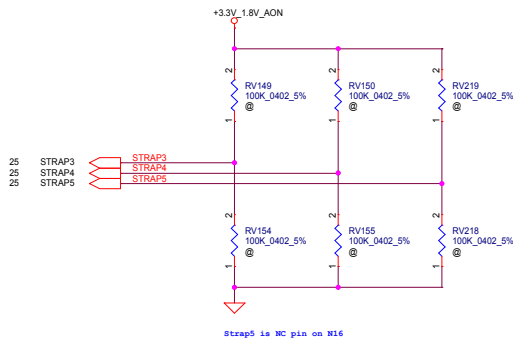






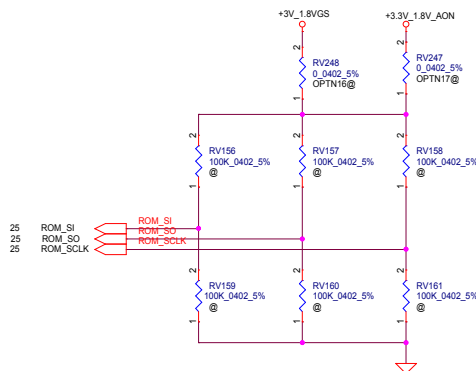


GPU	FB Memory (GDDR5)		RAMCFG[4:0]	STRAP2	STRAP1	STRAP0
8Gb	Samsung 8Gb	K4G80325FB-HC28	0 (0x0000)	L	L	L
	Micron 8Gb	MT51J256M32HF-70:A	1 (0x0001)	L	L	H
	Hynix 8Gb	H5GC8H24MJR-R0C	2 (0x0010)	L	H	L



STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

- 1: SMB\_ALT\_ADDR ENABLE  
0: SMB\_ALT\_ADDR DISABLE
- 1: DEVID\_SEL REBRAND  
0: DEVID\_SEL ORIGINAL
- 1: PCIE\_CFG LOW POWER  
0: PCIE\_CFG HIGH POWER
- 1: VGA\_DEVICE ENABLE  
0: VGA\_DEVICE DISABLE



	ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]
N17S-G1	H	H	M	0000
N16S-GTR				

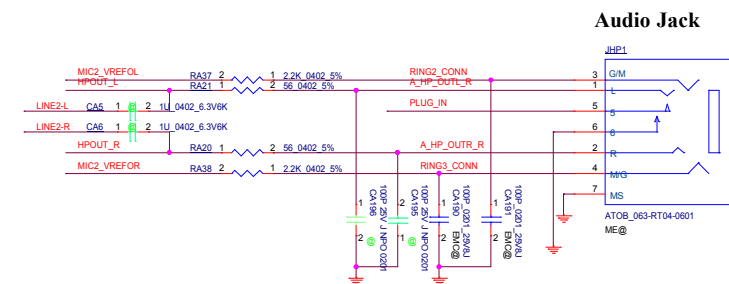
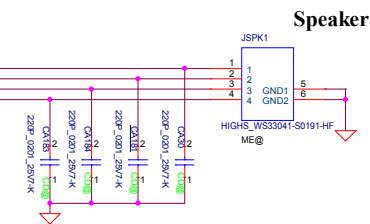
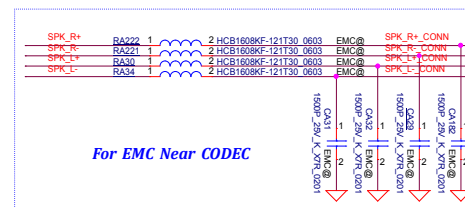
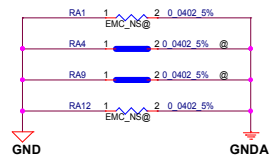
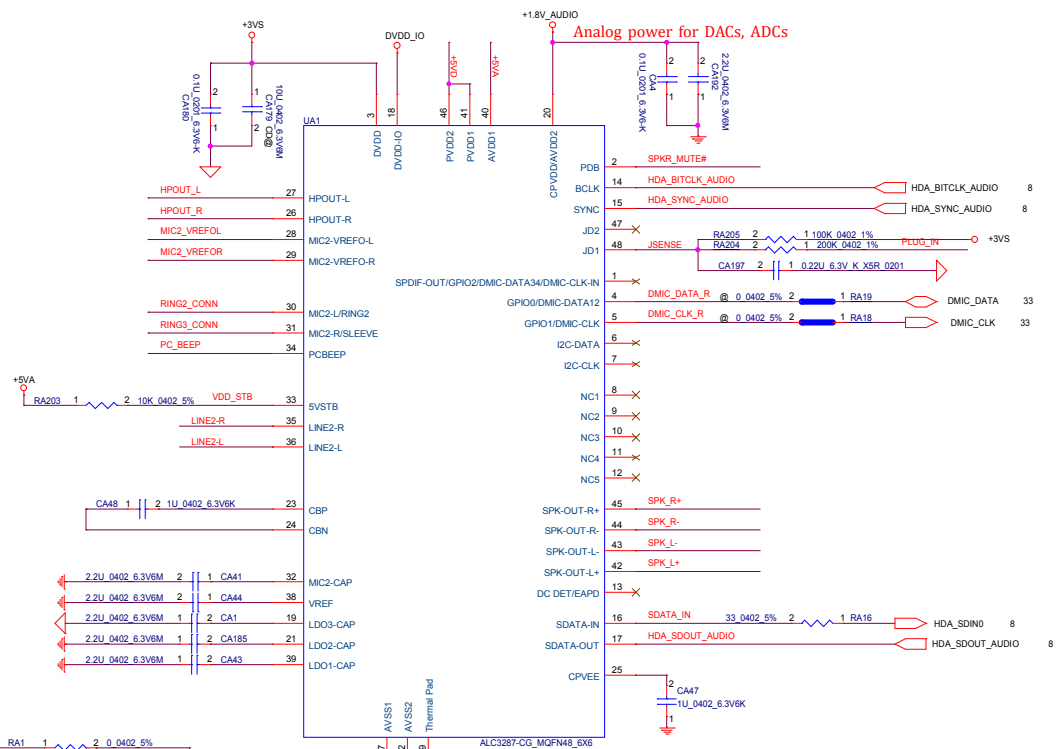
1:ENABLE 0:DISABLE  
SOR0/1/2/3 DISABLE


DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

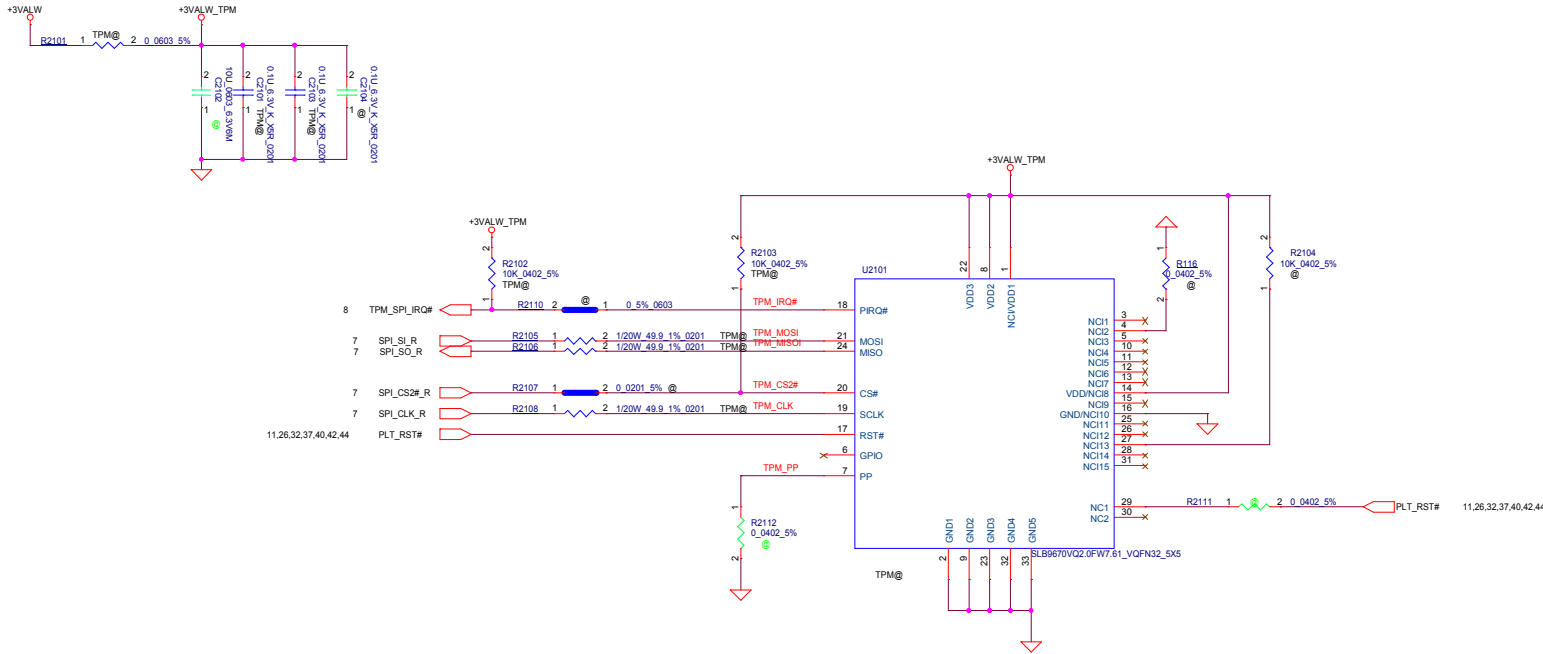
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



Security Classification				LC Future Center Secret Data				Title		
Issued Date		2018/03/15		Deciphered Date		2019/03/14		<b>Codec ALC3287</b>		
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Size		Document Number				<b>FG540/FG740</b>				Rev
Date		Thursday, December 13, 2018				30 of 60				0.1

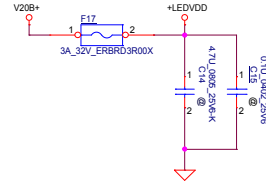
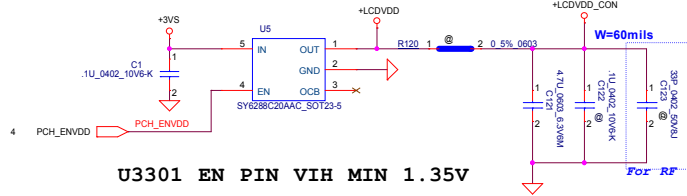




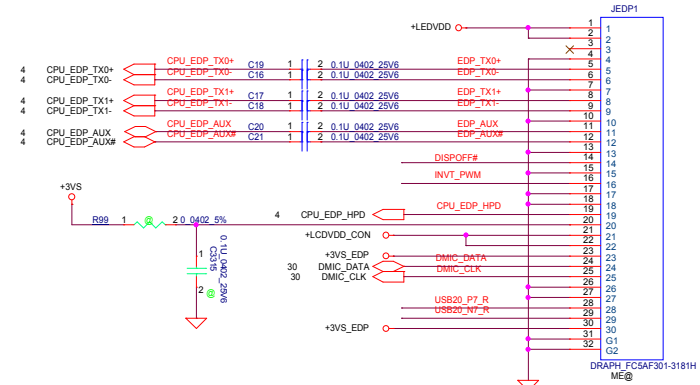
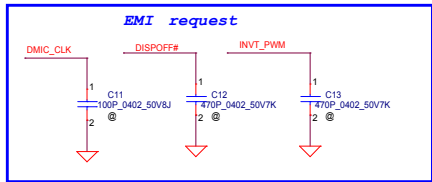
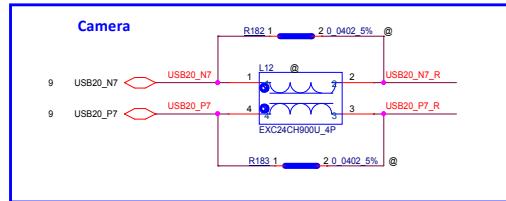
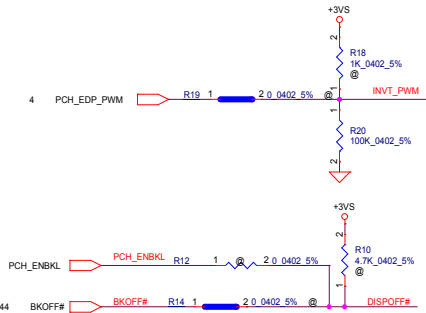
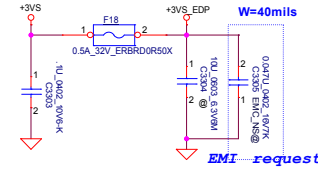
TABLE

Pin No	TCG PTP Spec (v38)	Infineon SLB9670VQ2.0 FW 7.61	ST Micro ST33HTPH2E32AHB4	Nuvoton NPCT750LABYX	NATIONZ Z3H330TC
1	VDD	NC/VDD	NC	VSB	VDD
2	GND	GND	NC	NC	GND
3	GPIO	NC	NC	NC	NC
4	GPIO	NC	NC	PP/GPIO6	NC
5	NC	NC	NC	NC	NC
6	VNC/GPIO	GPIO	GPIO	GPIO3	NC
7	GPIO/VDD	PP	PP	NC	PP
8	VDD	VDD	NC	VHIO	VDD
9	GND	GND	NC	NC	GND
10	VNC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC
13	VNC/GPIO	NC	NC	GPIO4	NC
14	VDD	NC/VDD	NC	NC	VDD
15	NC	NC	NC	NC	NC
16	GND	NC/GND	NC	GND	GND
17	SPI_RST#	RST#	SPI_RST#	PLTRST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	CS#	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI	MOSI	MOSI/GPIO7	MOSI
22	VDD	VDD	VPS	VHIO	VDD
23	GND	NC	NC	GND	GND
24	MISO	MISO	MISO	MISO	MISO
25	NC	NC	NC	NC	NC
26	NC	NC	NC	NC	NC
27	NC	NC	NC	NC	NC
28	NC	NC	NC	NC	NC
29	VNC/GPIO	NC	NC	SDA/GPIO0	NC
30	VNC/GPIO	NC	NC	SCL/GPIO1	NC
31	VNC	NC	NC	NC	NC
32	GND	GND	NC	NC	GND

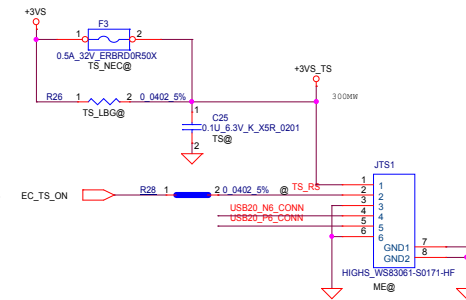
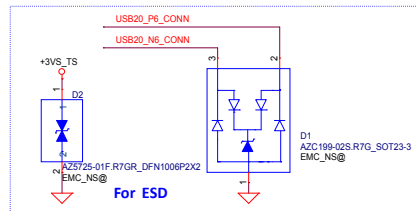
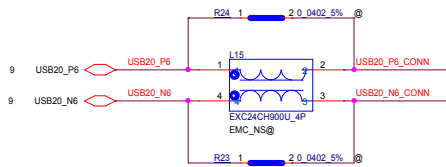
## LCD POWER CIRCUIT

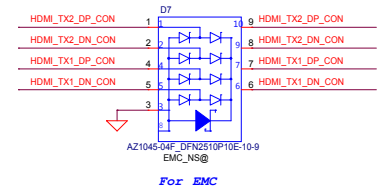
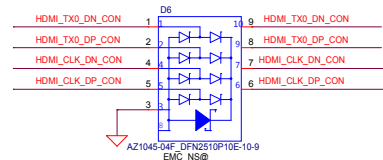
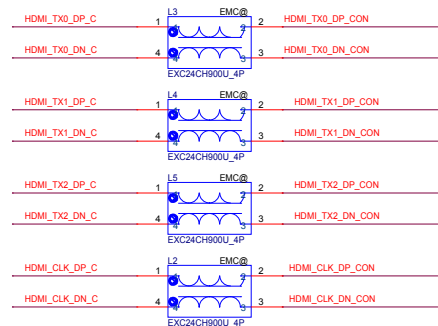
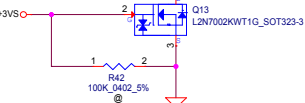
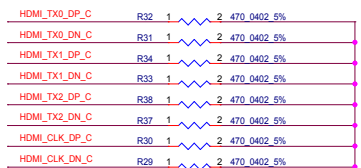
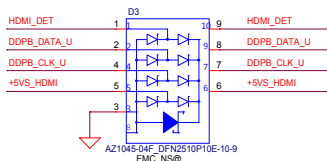
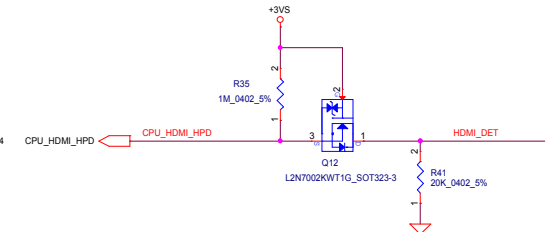
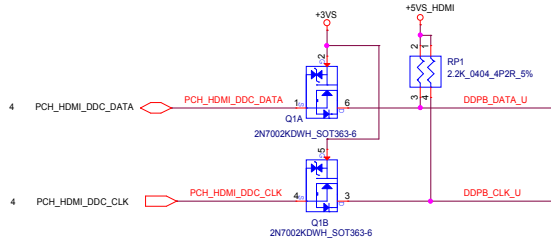
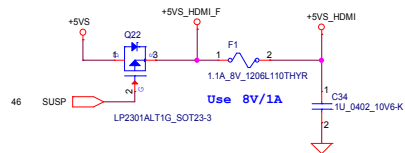
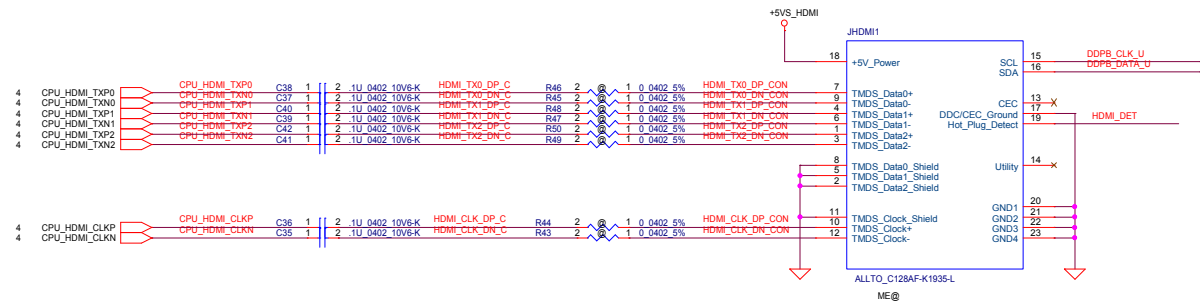


## CMOS Camera



## Touch Screen











+3VALW TO +3VALW\_LAN

+3VALW\_LAN rising time (10%~90%)  
0.5ms < t<sub>pe</sub> < 100ms

Need short

width : 40 mils

Close to Pin11 Close to Pin32 Close to Pin11 Close to Pin32

manual change the Codec PN to RTL8111GUL-CG

For RTL8111GUL(SWR mode, reserved)  
For RTL8111H (LDO mode)

Layout Note: LL1 must be  
within 200mil to Pin24,  
CL15,CL16 must be within  
200mil to LL1  
+LAN\_REGOUT: Width =60mil

2018/01/24: add A25815-01F.R7GR for  
RTL8111H Lan Surge issue

04/03 add A25815\_brom

Security Classification	LC Future Center Secret Data
Issued Date	2018/03/15
Deciphered Date	2019/03/14

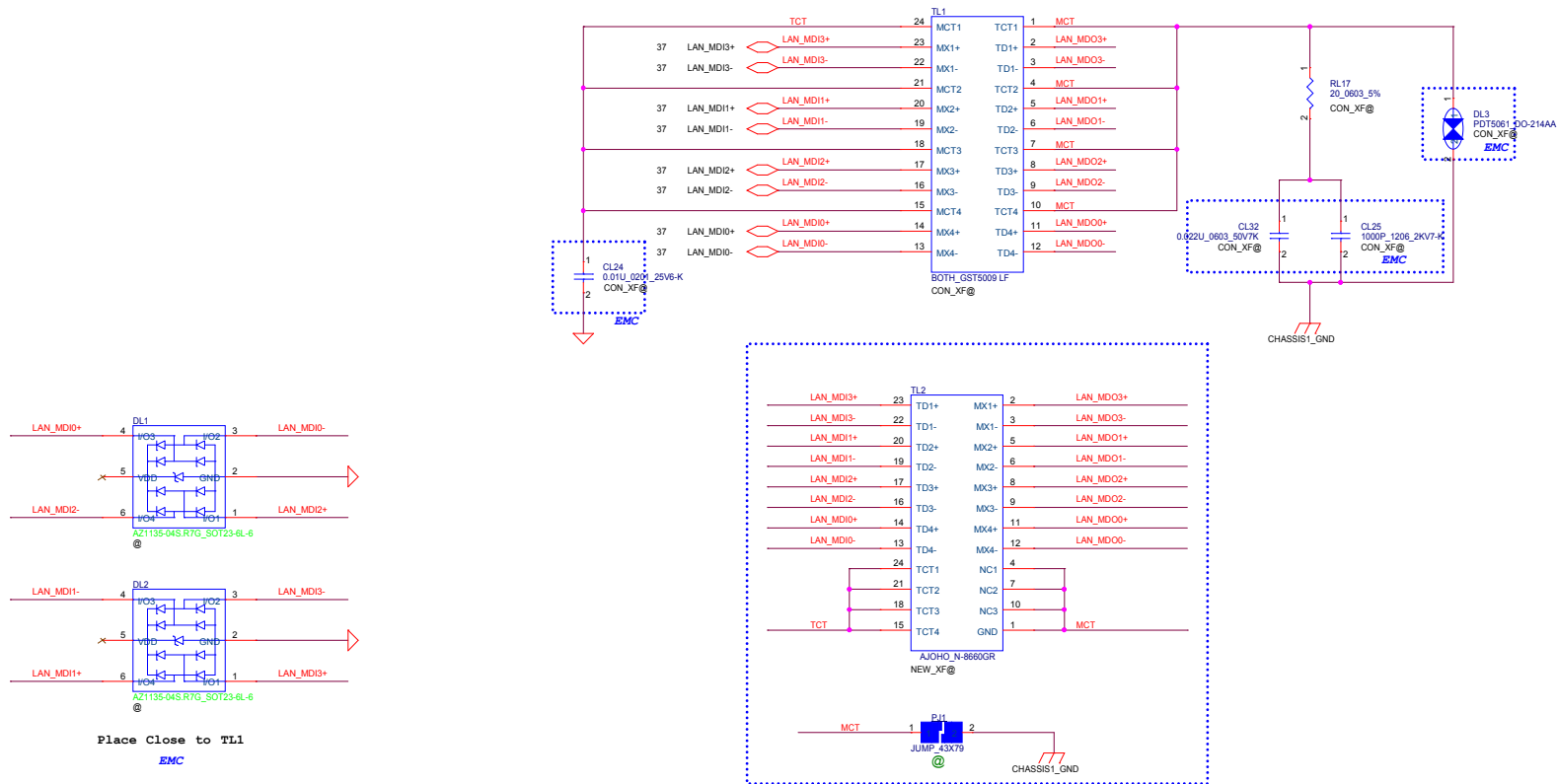
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Title  
**LAN\_RTL8111H\_CG**

Size Document Number  
**FG540/FG740**

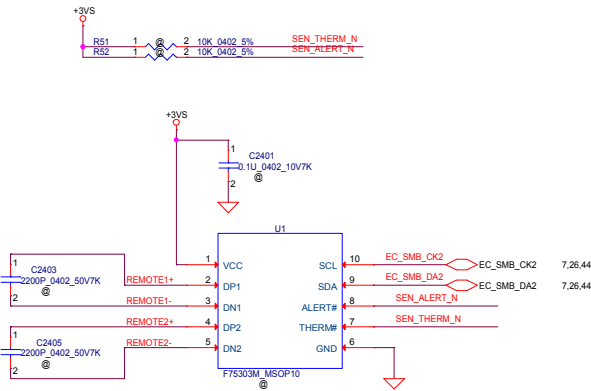
Date: Tuesday, December 11, 2018 Sheet 37 of 60

Rev  
0.1

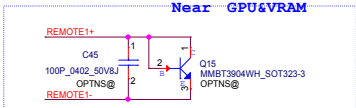


SMSC thermal sensor  
placed near DIMM

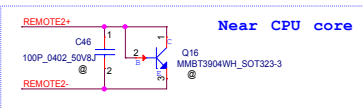
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



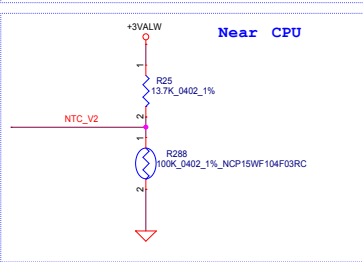
Near GPU&VRAM



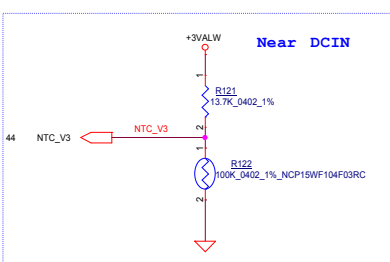
Near CPU core



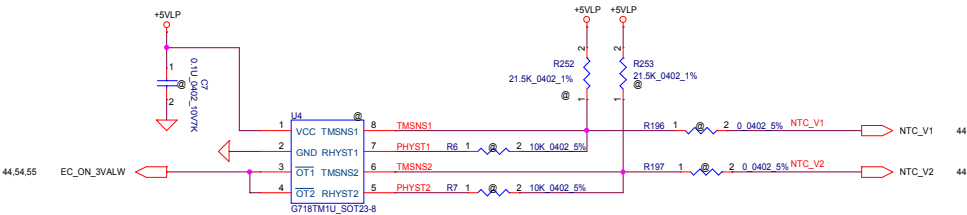
Near CPU



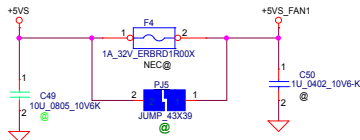
Near DCIN



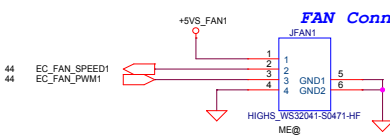
HW thermal sensor



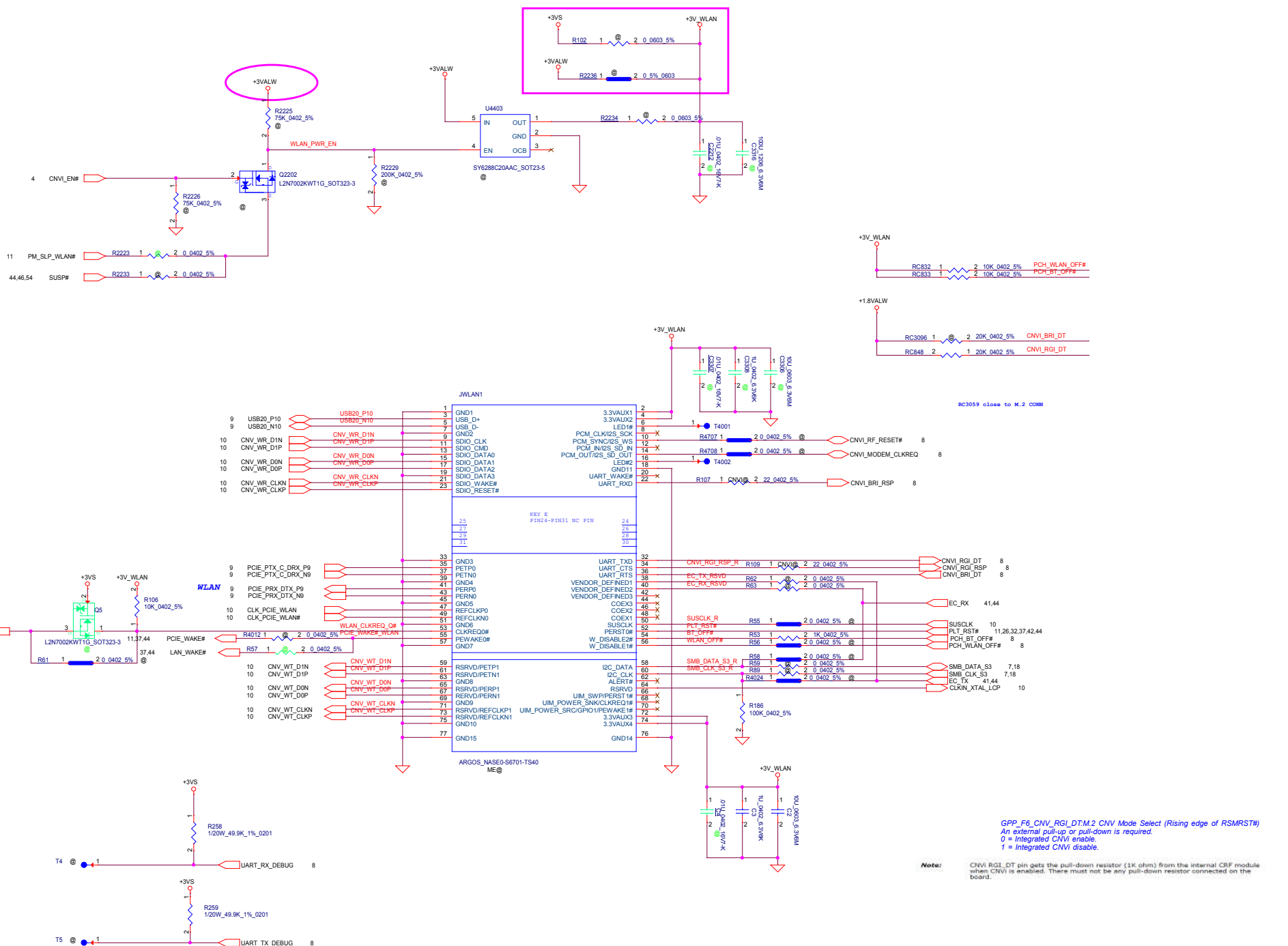
over temperature threshold:  
RSET=3\*RTMH  
92+/-30C  
Hysteresis temperature threshold.  
RHYST=(RSET\*RTML)/(3\*RTML-RSET)  
56+/-30C




FAN Conn

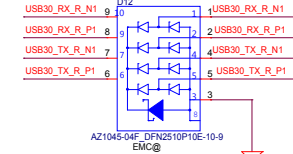
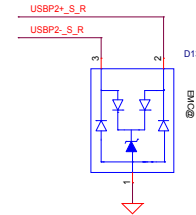
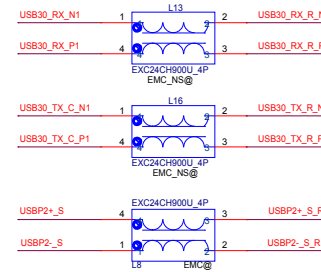
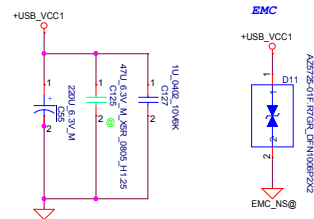
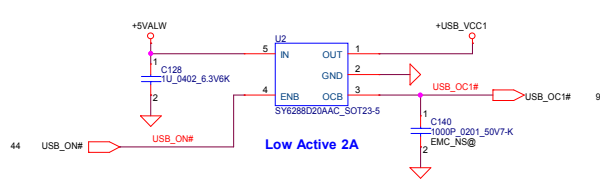


### *Mini-Express Card(WLAN/WiMAX)*

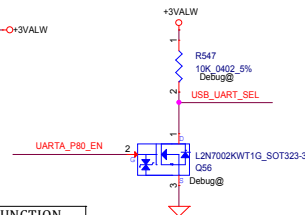
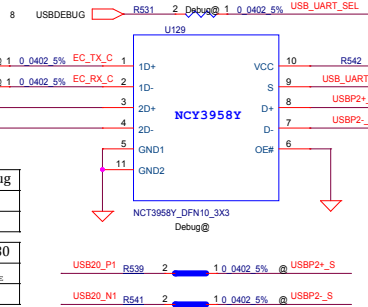


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Date    Wednesday, December 13, 2018    7:00 AM								Rev    0.1	

## LEFT SIDE USB3.0 PORT x2

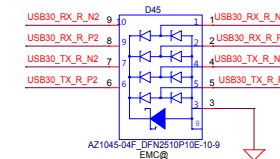
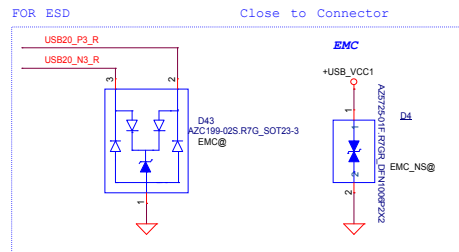
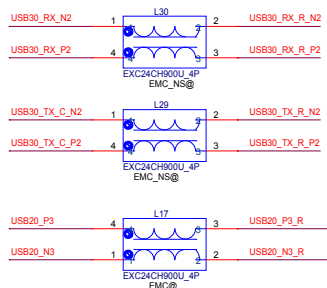
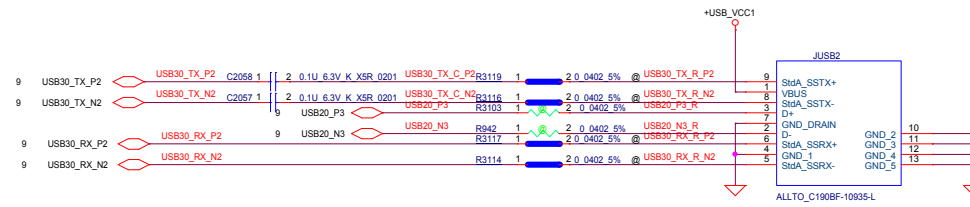
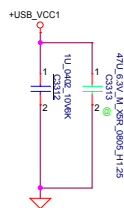
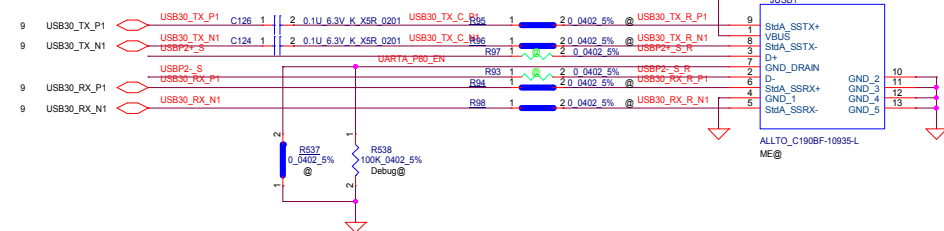


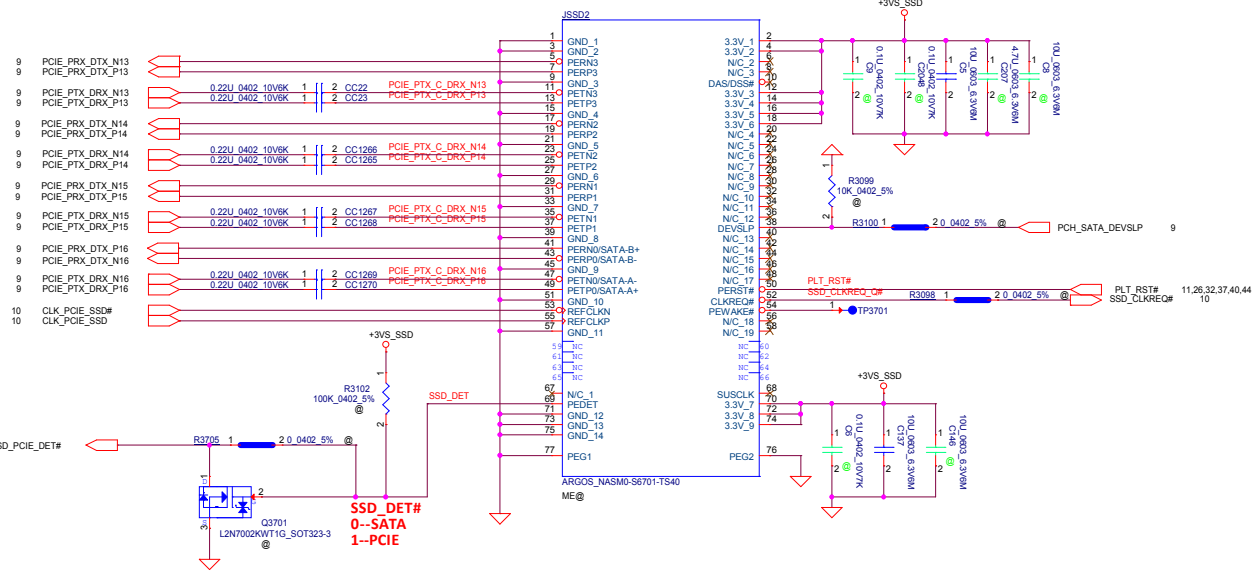
## For USB Debug Function



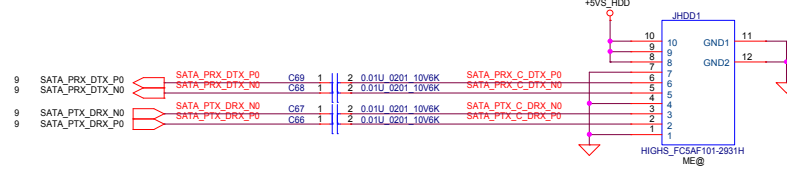
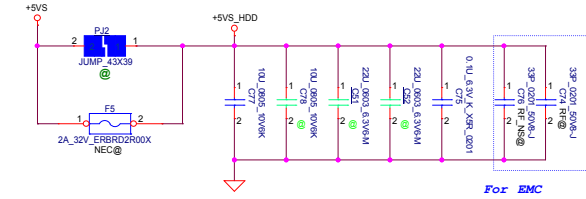
OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/+) to D(-/-)
L	H	D(-/-) to D(+/+)

04/02 add USB debug function bron

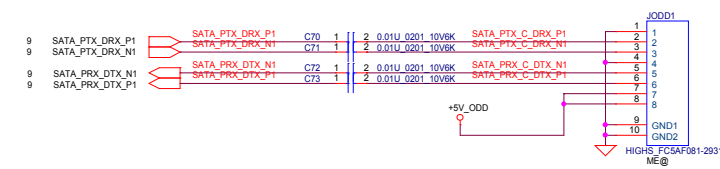
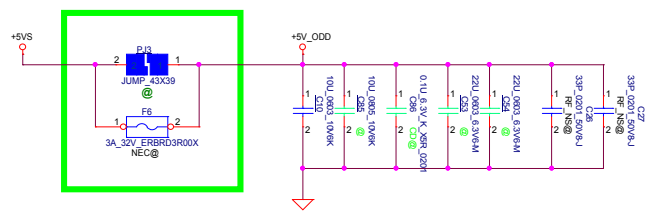


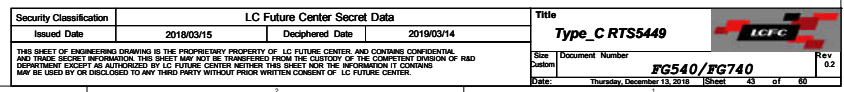


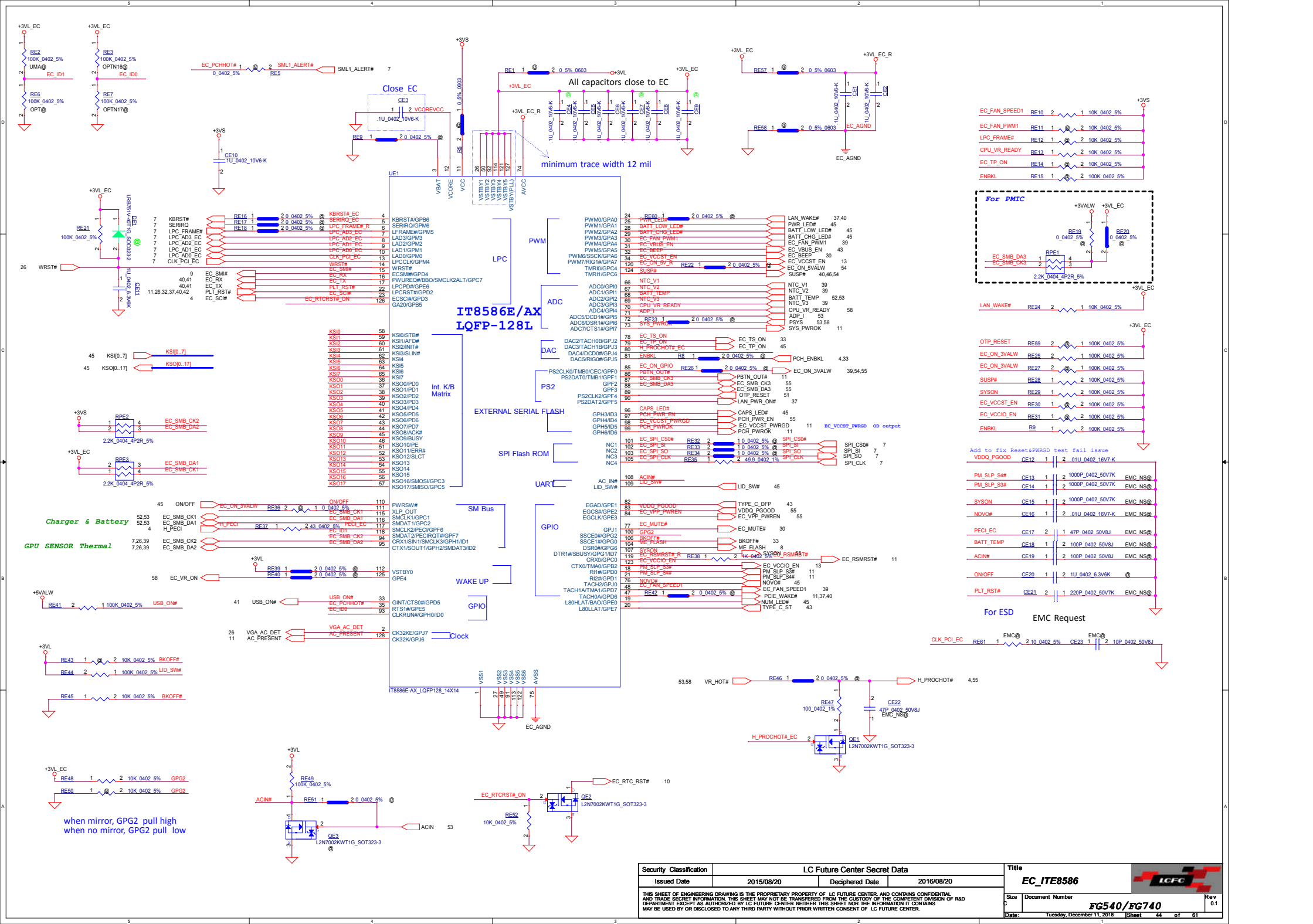
# SATA HDD Conn.




# ODD Conn.



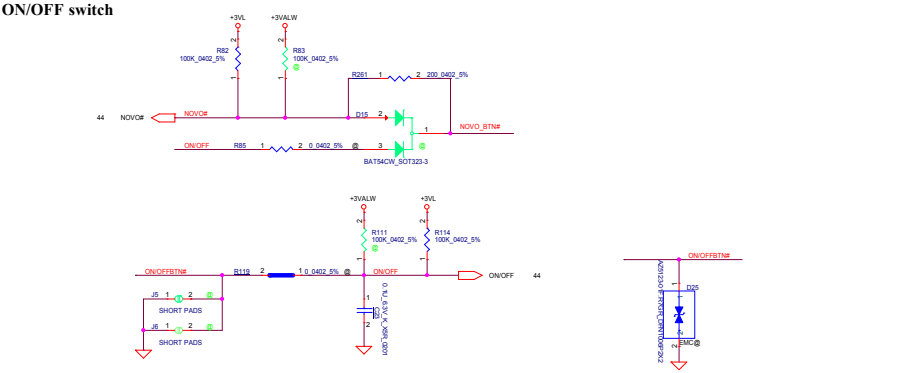




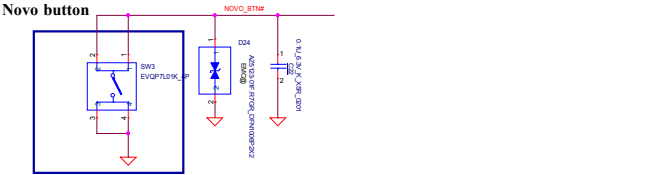
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2015/08/20		2016/08/20				
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				Date: Tuesday, December 11, 2016 Sheet 44 of 61		



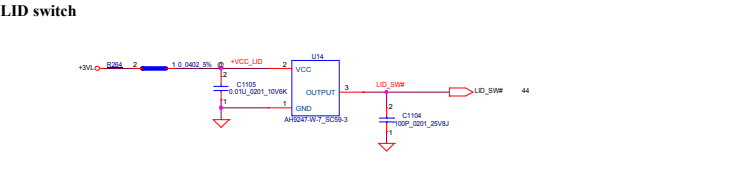
ON/OFF switch



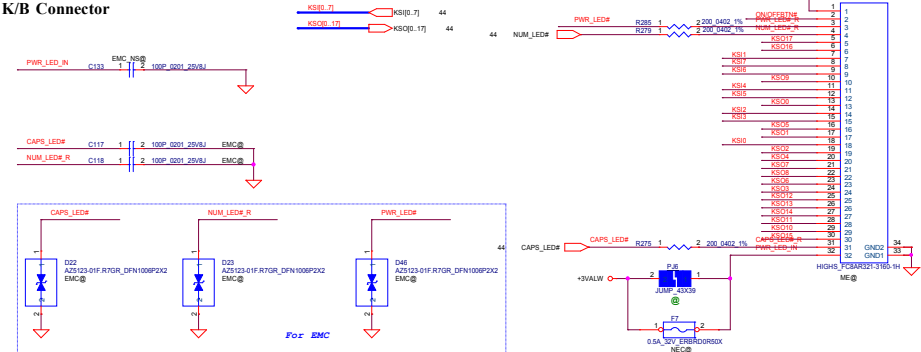
Novo button



LID switch



K/B Connector



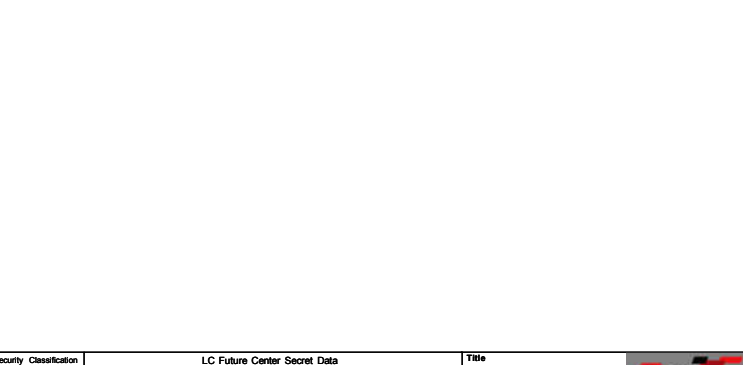
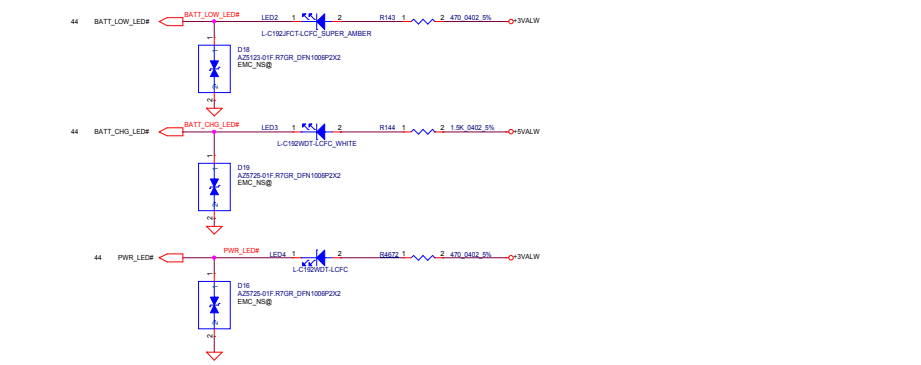
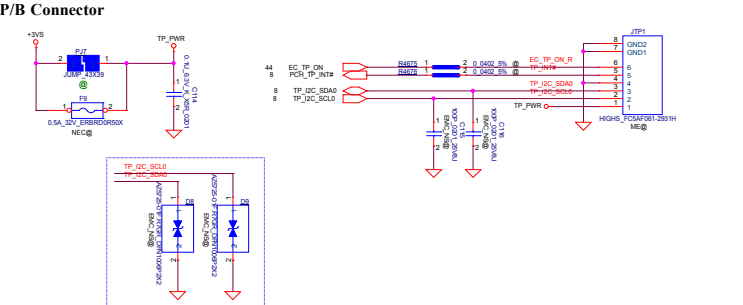
KB Backlight Connector

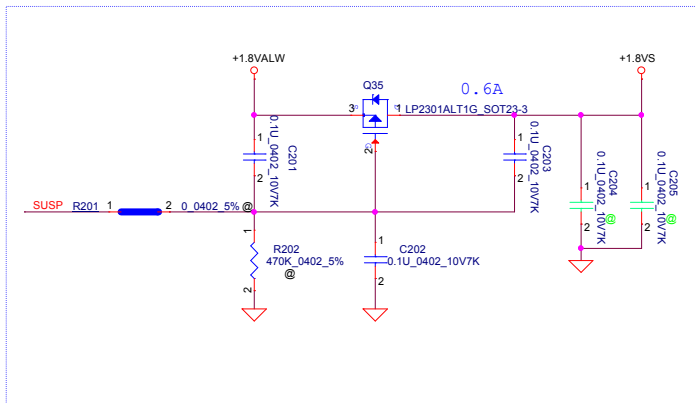
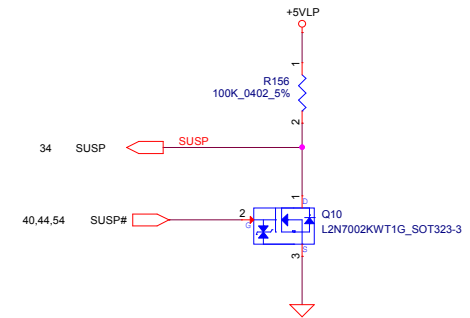
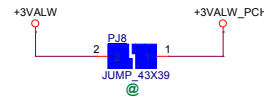


Finger Print Connector



TP/B Connector

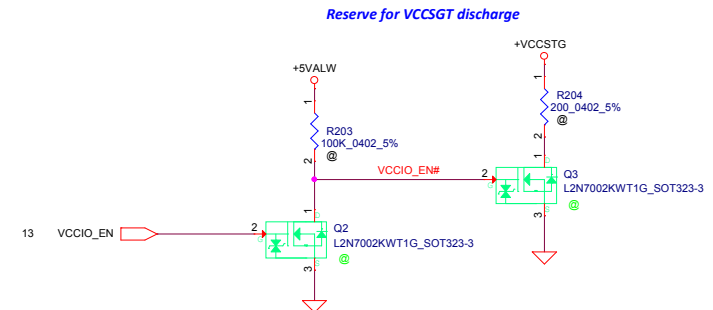




For DisCharge



08/29: Need double check enable signal and the resistance

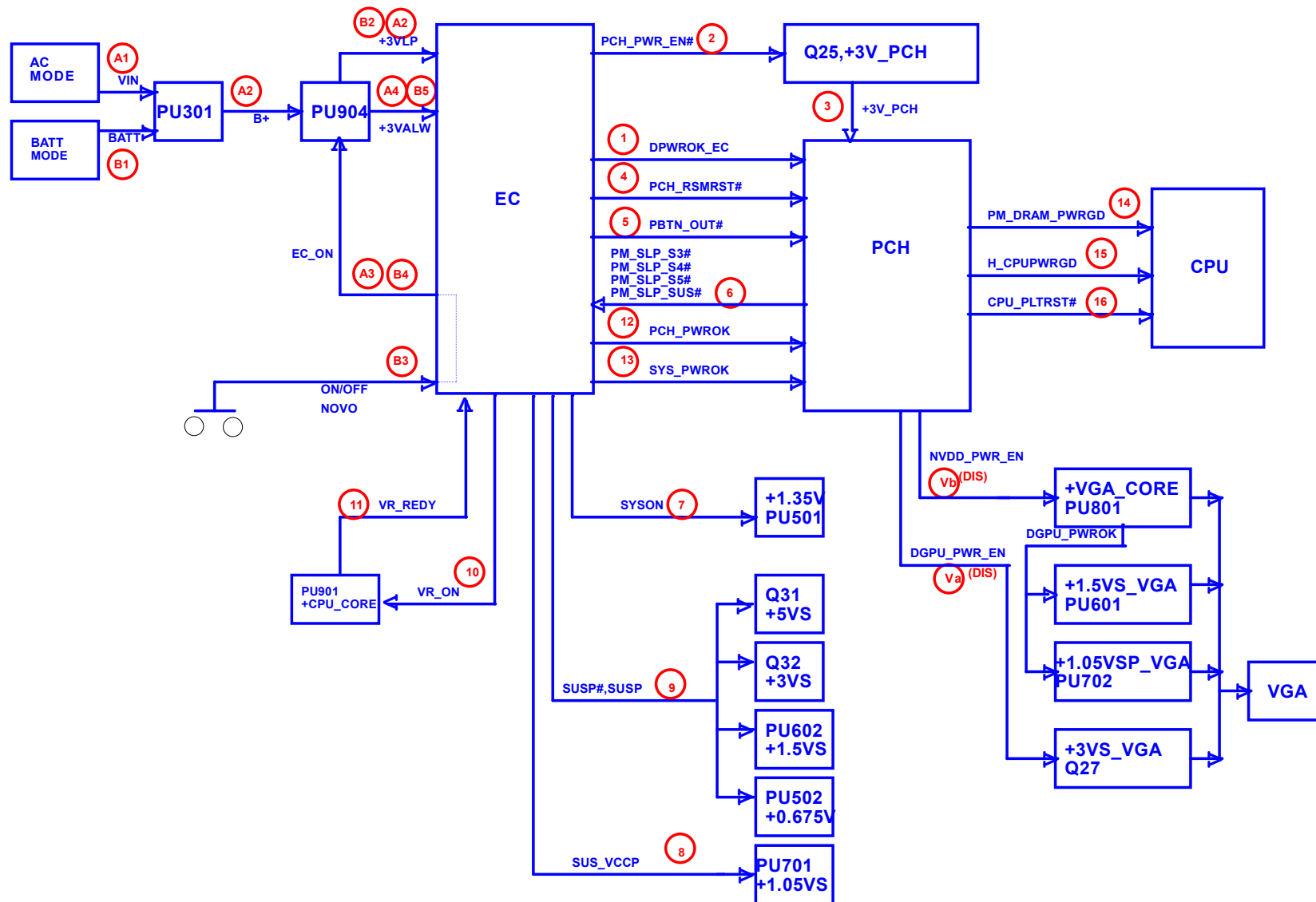


## 12.1.4 VccSTG Rail Discharge Requirements

As long as VccST and VccSTG are power gated separately, the following requirements are critical to prevent system failure on Whiskey Lake:

1. VccSTG should have a discharge circuit, either integrated into its load switch or externally on the motherboard. The recommended nominal  $R_{\text{discharge}} \leq 300\Omega$  to GND. The discharge circuit should be activated when the VccSTG load switch is disabled.
2. If VccST/VccPLL has a discharge circuit, either integrated into its load switch or externally on the motherboard, then VccSTG nominal  $R_{\text{discharge}} \leq \text{VccST/VccPLL } R_{\text{discharge}}$ .
3. The total capacitance on VccSTG  $\leq$  total capacitance on VccST/VccPLL.

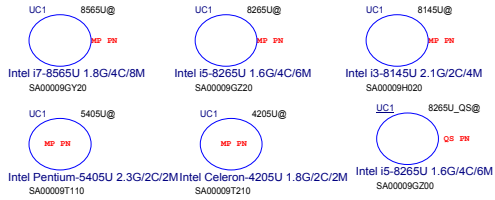
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Issued Date	2015/08/20	Deciphered Date	2016/08/20	DC V TO VS INTERFACE	
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				Sheet	46 of 61



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Title		Power sequence block		
Size	Document Number	FG540/FG740		Rev 0.1
Date:	Tuesday, December 11, 2018	Sheet	47	of 61

### CPU



### DRAM\_Micron



### DRAM\_Hynix



### DRAM\_Samsung



### SO\_DIMM only



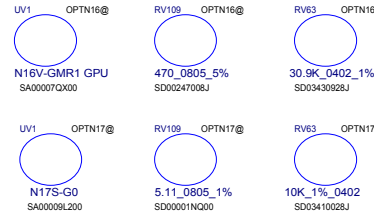
### LAN Chip



### PCB\_MB



### GPU



### VRAM\_Samsung

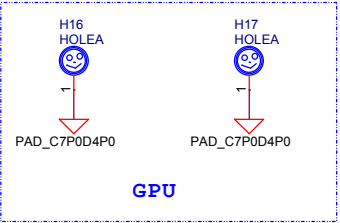
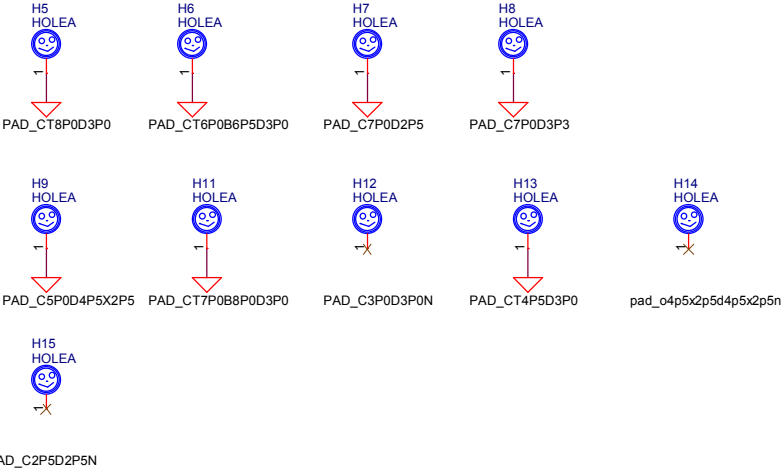
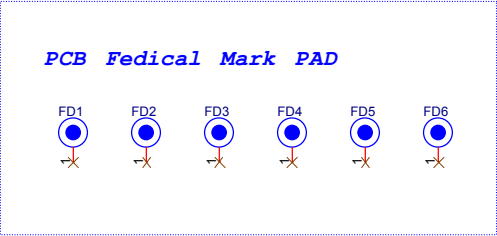
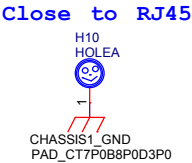
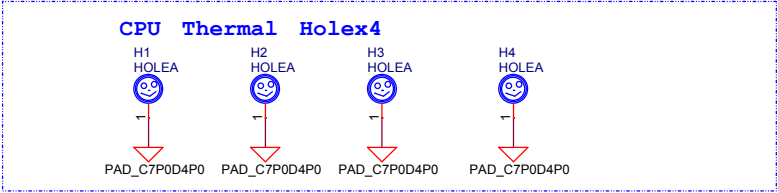



### VRAM\_Micron

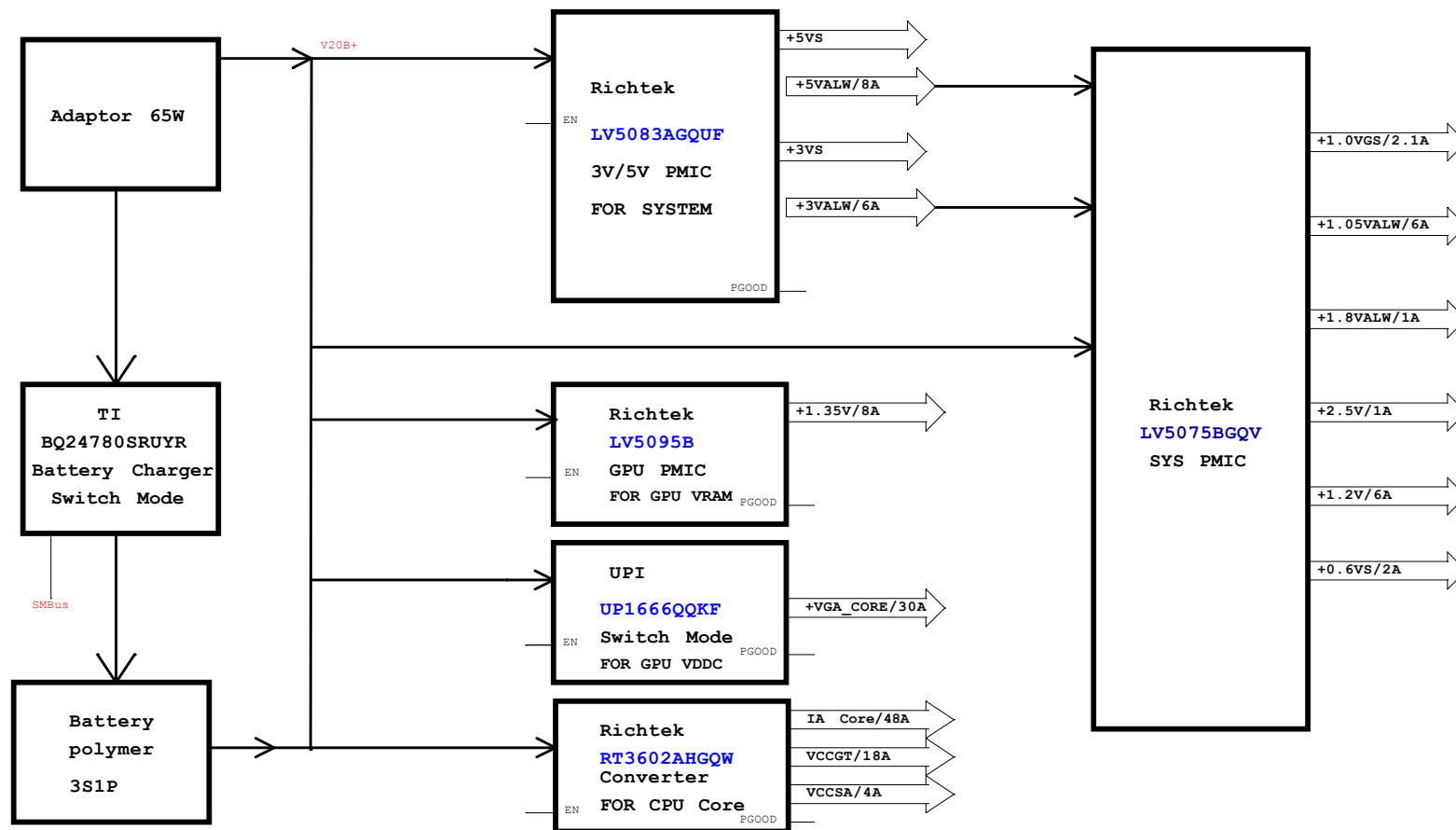


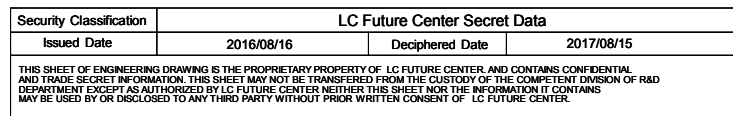
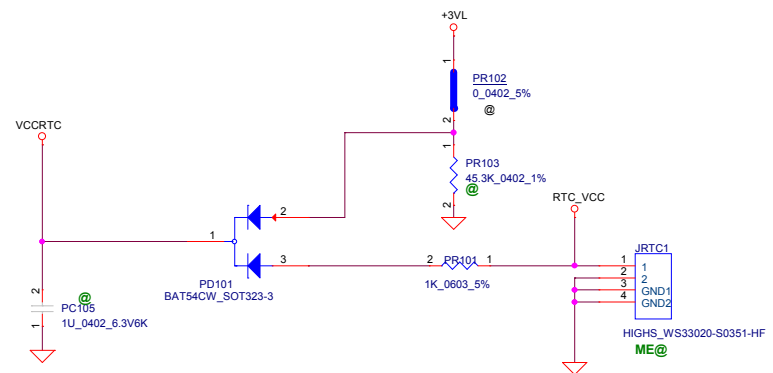
### VRAM\_Hynix




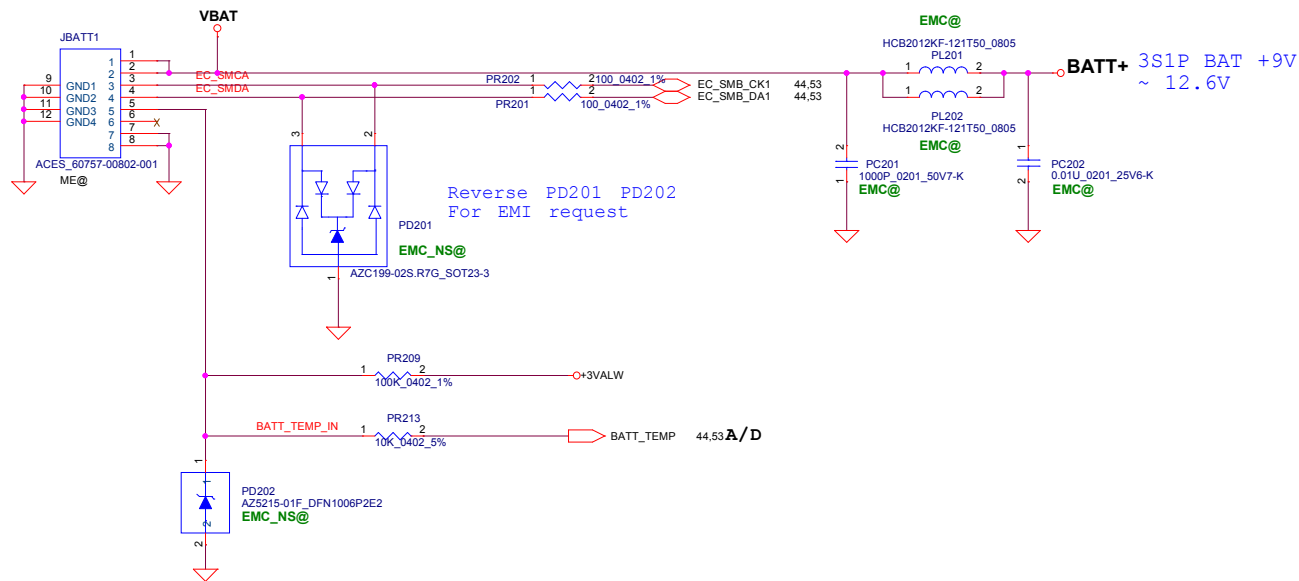




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	FG540/FG740				0.1		
Date:		Tuesday, December 11, 2018		Sheet 49 of 61			





Title		<b>PWR-DCIN / RTC charger</b> 	
Size Custom	Document Number	<b>FG540/FG740</b>	
Date:	Tuesday, December 11, 2018	Sheet	51 of 61
		Rev	0.1



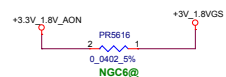
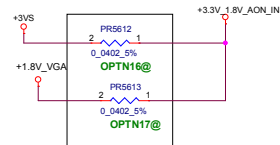
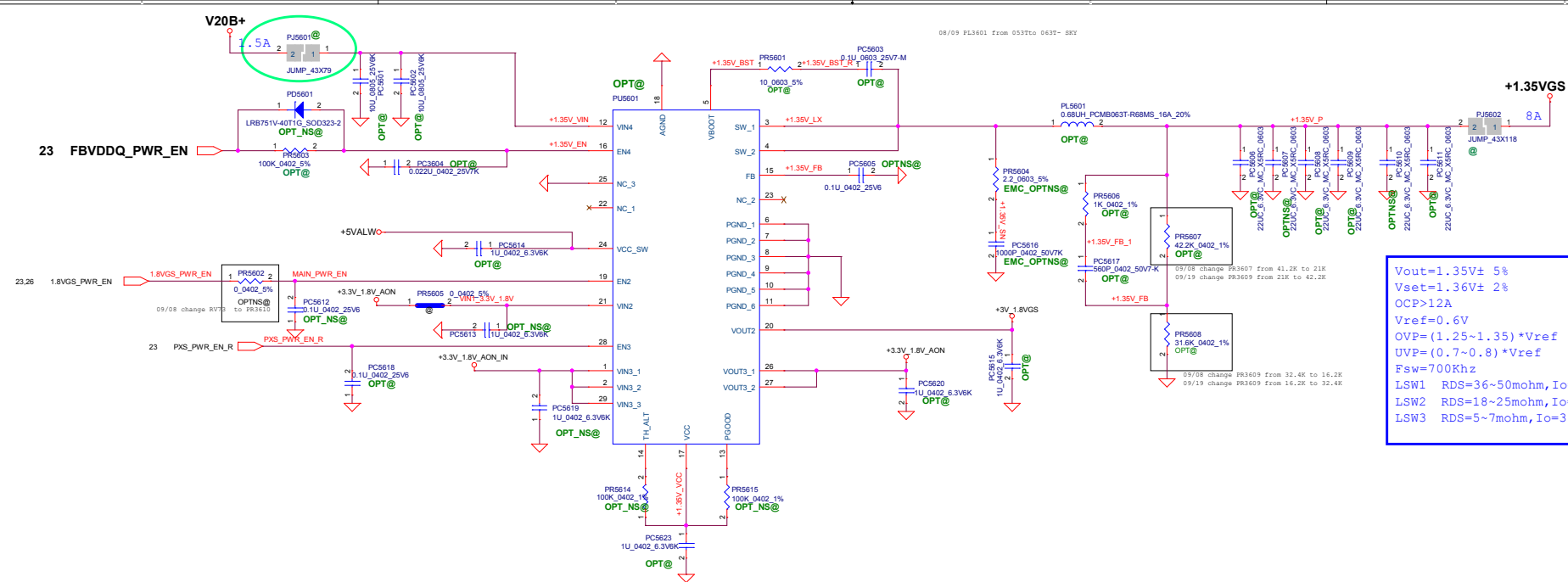
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				Size		Document Number		Rev	
				Custom		FG540/FG740		1.0	
				Date:		Tuesday, December 11, 2018		Sheet 52 of 60	



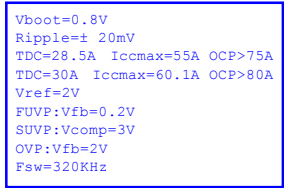









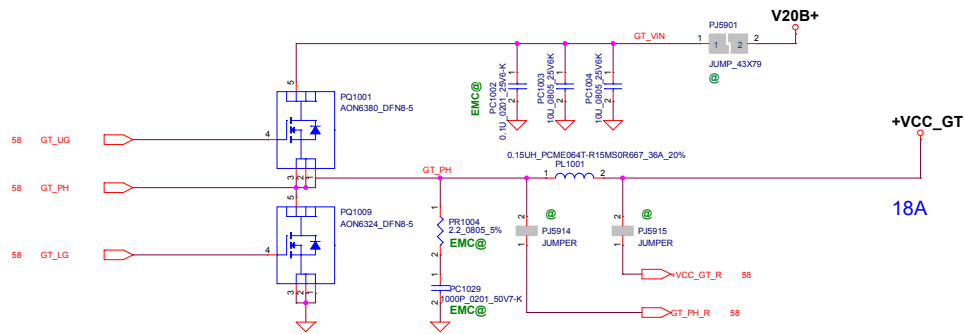
RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM



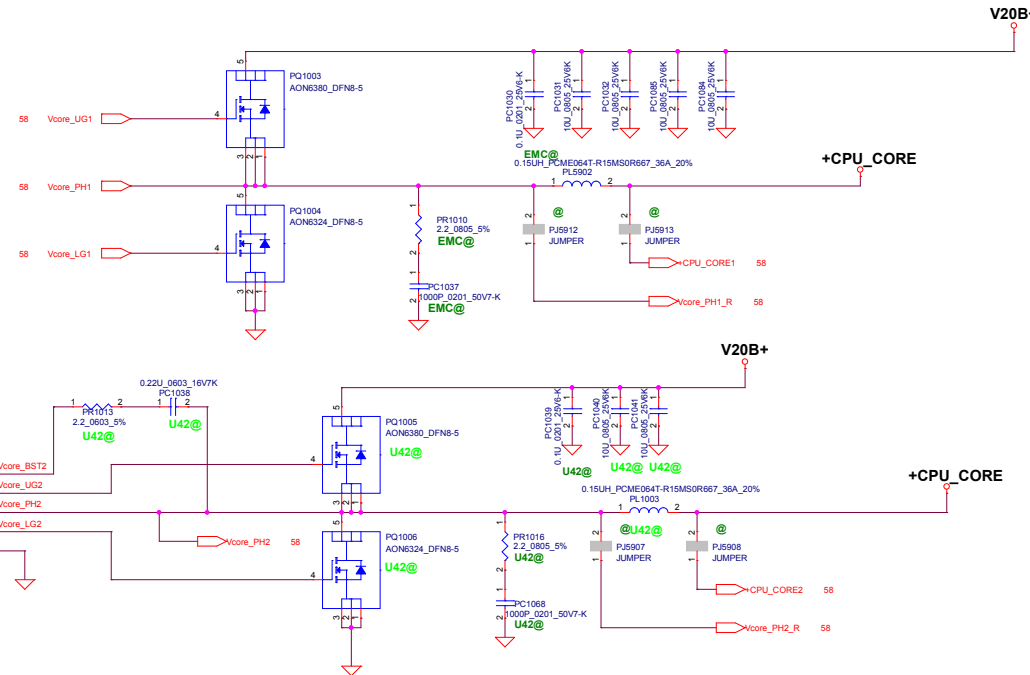
UPI\_OPT@ : for UP1666  
RT\_OPT@ : for RT8816A

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Issued Date	2015/08/20	Deciphered Date	2016/08/20	PWR-VGA_CORE		
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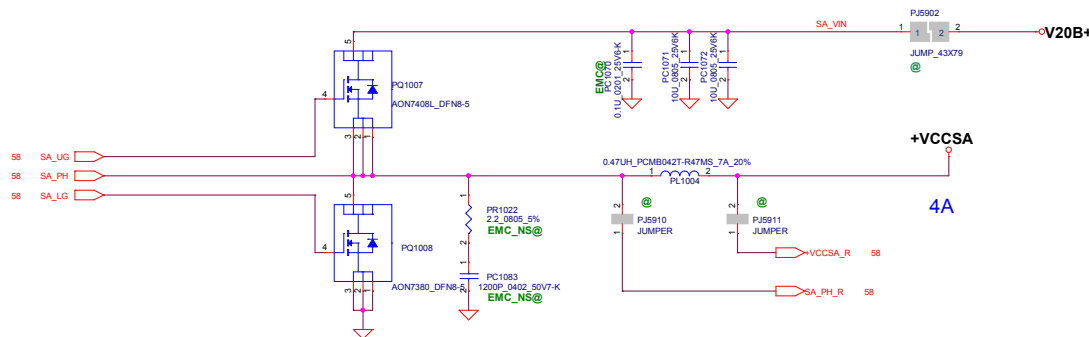
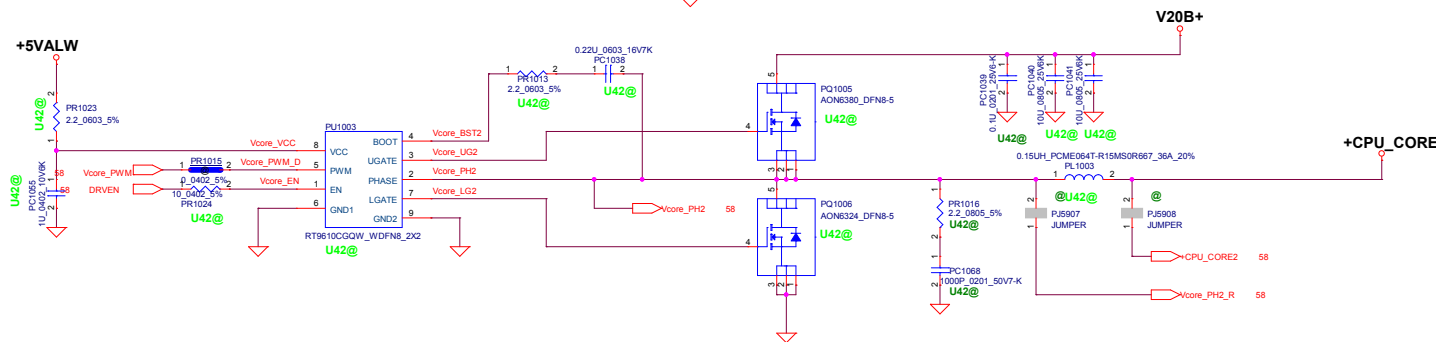


Vboot=0V Loadline=3.1mΩ  
 Ripple=+30mV/-10mV (0A~0.5A)  
 Ripple=± 10mV (0.5A~TDC)  
 Ripple=± 15mV (TDC~Iccmax)  
 TDC=18A Iccmax=31A OCP=37A  
 OVP=VID+370mV~VID+430mV  
 Max Overshoot:70mv/10us  
 UVP=VID-370mV~VID-225mV  
 Fsw=550Khz

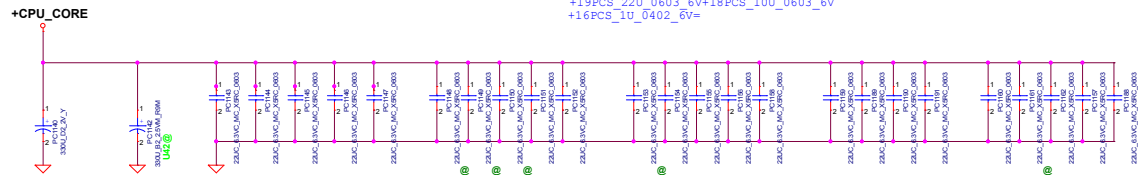


U22 :21A  
 U42: 48A

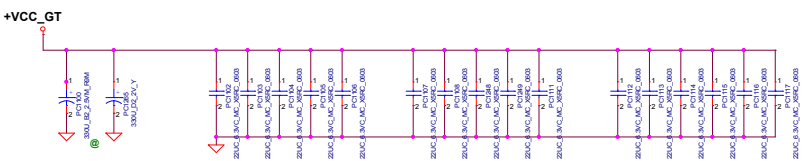
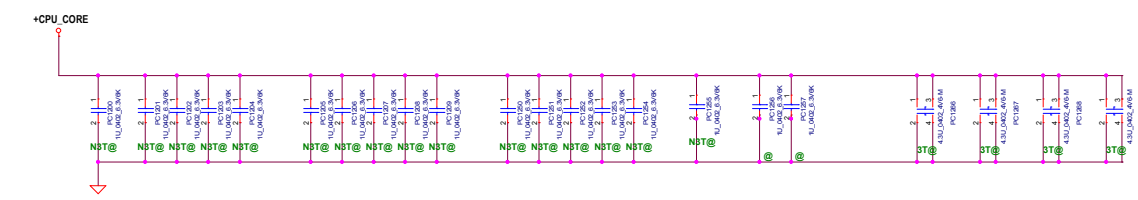
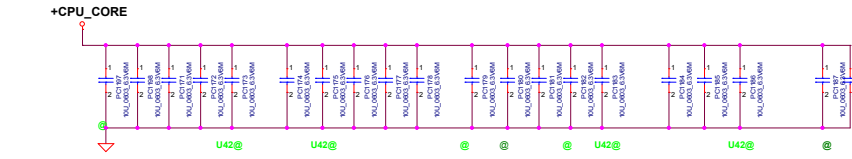
Vboot=0V Loadline=1.8mΩ  
 Ripple=+30mV/-10mV (0A~0.5A)  
 Ripple=± 10mV (0.5A~TDC)  
 Ripple=± 15mV (TDC~Iccmax)  
 TDC=21A/48A Iccmax=32A/70A  
 OCP=37A / 74A  
 Max Overshoot:70mv/10us  
 OVP=VID+370mV~VID+430mV  
 UVP=VID-370mV~VID-225mV  
 Fsw=550Khz



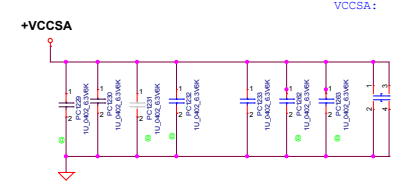
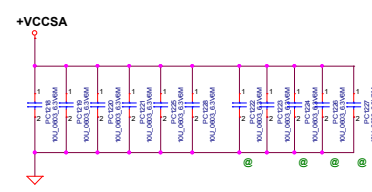
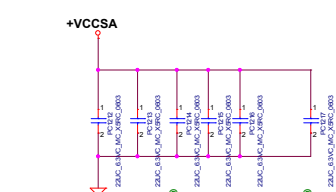
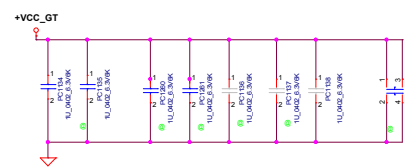
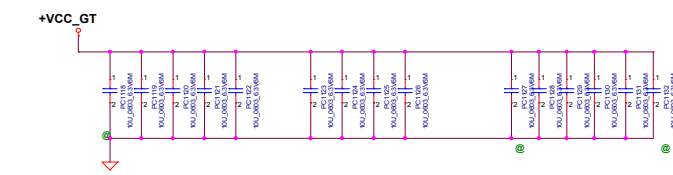
Vboot=0V Loadline=10.3Ω  
 Ripple=+30mV/-10mV (0A~0.5A)  
 Ripple=± 10mV (0.5A~TDC)  
 Ripple=± 15mV (TDC~Iccmax)  
 TDC=4A Iccmax=4.5A OCP=7A  
 Max Overshoot:70mv/10us  
 OVP=VID+370mV~VID+430mV  
 UVP=VID-370mV~VID-225mV  
 Fsw=550Khz



CPU\_CORE: 2PCS 330U B2 2V  
+19PCS 220 0603 6V+18PCS 100 0603 6V  
+16PCS 100 0402 6V=

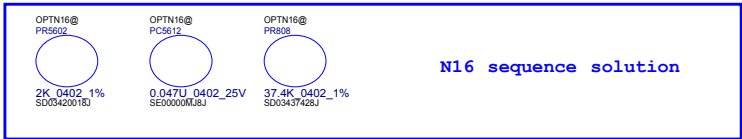
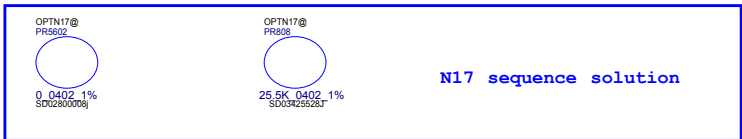
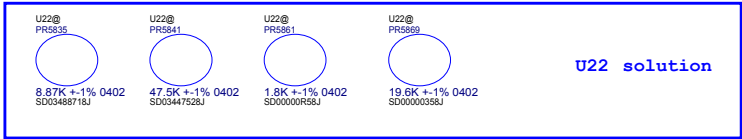
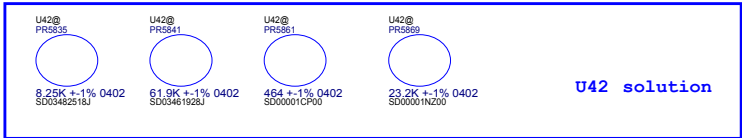
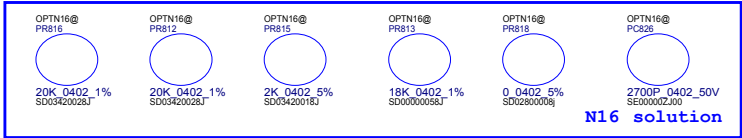
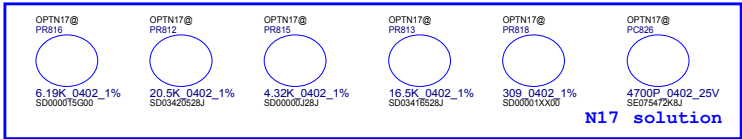
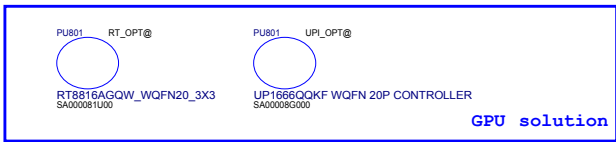


GT : 1PCS 220U B2 2.5V+ 1PCS 330U B2 2.5V  
+15PCS 220 0603 6V + 9PCS 100 0402 6V  
+2PCS 100 0402 6V=862U



VCCSA: 6PCS 22U 0603 6V  
+6PCS 100 0402 6V  
+2PCS 100 0402 6V=





Component	Value	N17	N16S-GTR
R1 (KQ )	PR816	6.19	20
R2 (KQ )	PR812	20.5	20
R3 (KQ )	PR815	4.32	2
R4 (KQ )	PR813	16.5	18
R5 (KQ )	PR818	0.309	0
C (nF)	PC826	4.7	2.7